Design Project - Ring Oscillator Design - TCES 421

Souleymane Dembele

July 19, 2023

Abstract

The main objective of this project is to design a ring oscillator using the IBM 0.18um CMOS (cmrf7sf) process. A ring oscillator is made up of odd number (N) of CMOS inverter stages connected in a circular chain. In this project, I will show the design and simulation results of the ring oscillator.

Introduction

In this project, I designed a ring oscillator using the IBM 0.18um CMOS (cmrf7sf) process. The ring oscillator is made up of odd number (N) of CMOS inverter stages connected in a circular chain. The ring oscillator meets the following requirements: a) Frequency of oscillation 1GHz within a margin of $\pm$ 100MHz. b) Design parameters to consider: N, Wn (NMOS transistor width), Wp (PMOS transistor width). c) DC Supply voltage to CMOS inverter do not exceed 1.8V. d) Verify and optimize the design using Cadence simulator showing output oscillating voltage waveform. Compute the frequency of oscillation. Using Cadence Virtuoso layout tool, generate the basic layout of the Ring Oscillator designed, run DRC/LVS and attach DRC/LVS output log.

Design/ Simulation Result

In this section I will show the design and simulation results of the ring oscillator. I started the design by creating a schematic of the ring oscillator. For

doing so, I first created a schematic of a single inverter represented in Figure 1. In Figure 2, from the single inverter, I created a symbol out of it as we learn during the quarter. Then I created a schematic of the ring oscillator using the inverter symbol represented in figure . I selected the analysis “tran”, stop time 100n, under Options/Time Step maxstep 0.7p. I run a transient simulation on the ring oscillator and got the results represented in Figure 5.

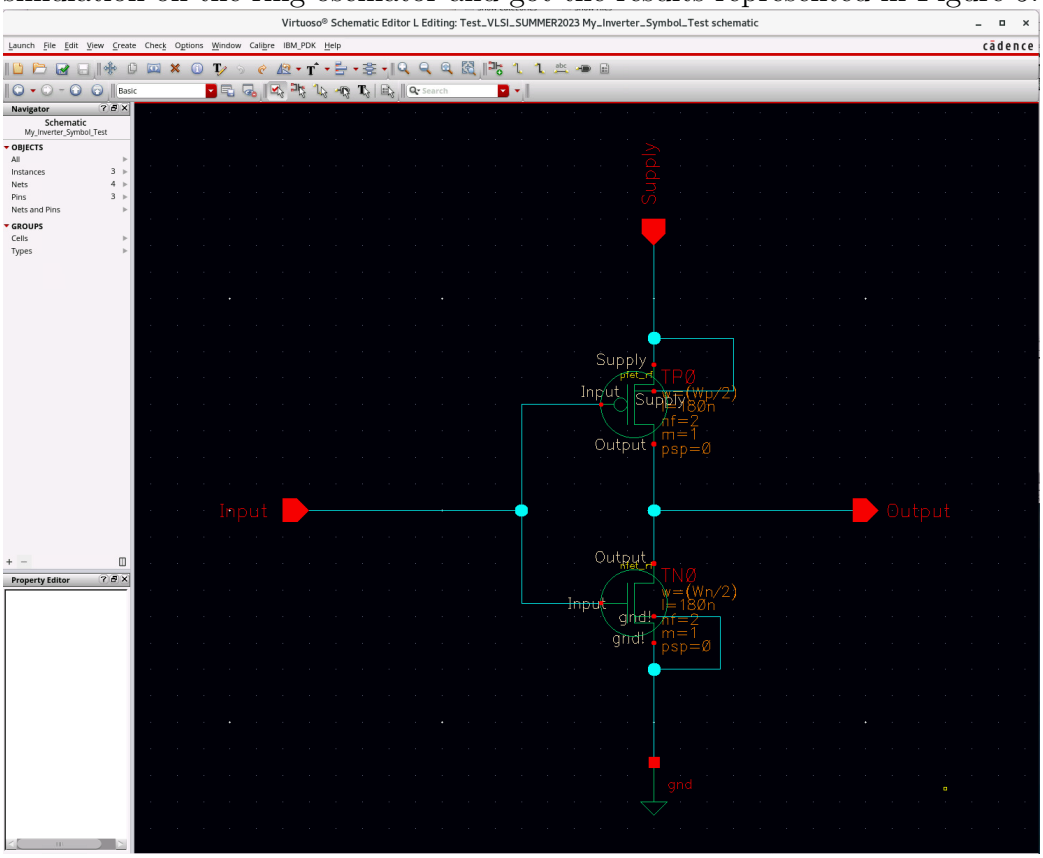

Figure 1: Represents the circuit schematic for a single inverter.

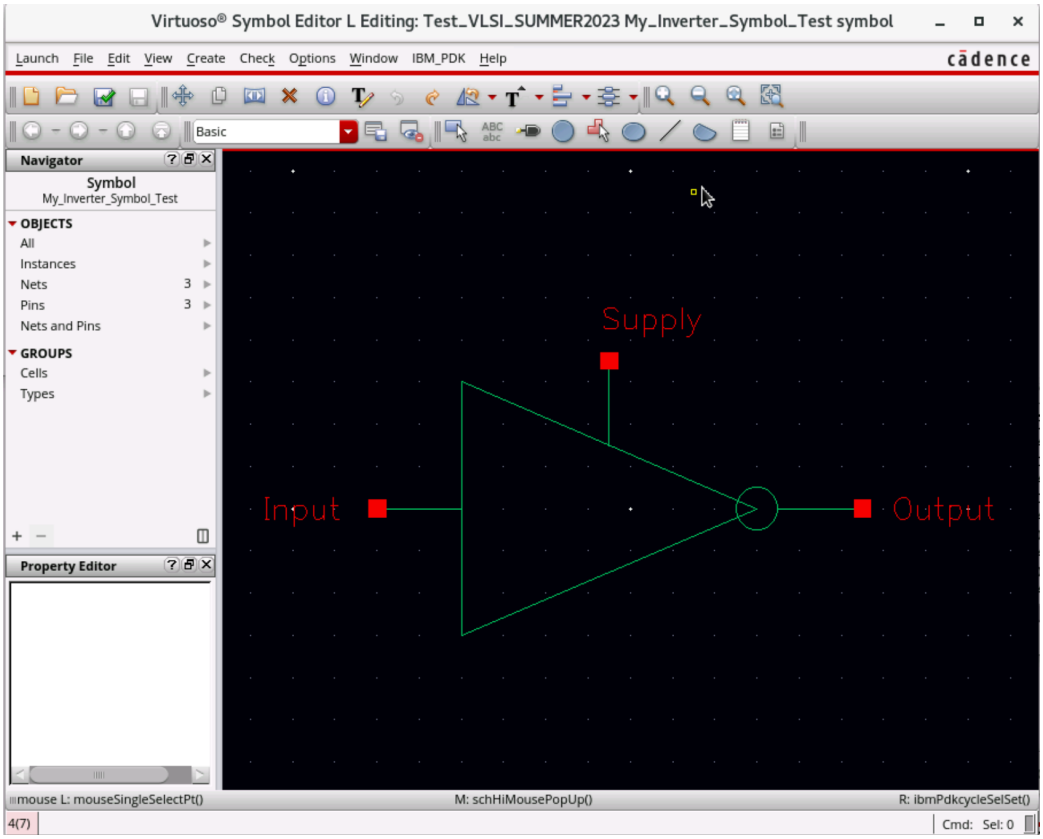

Figure 2: Represents the symbol of a single inverter.

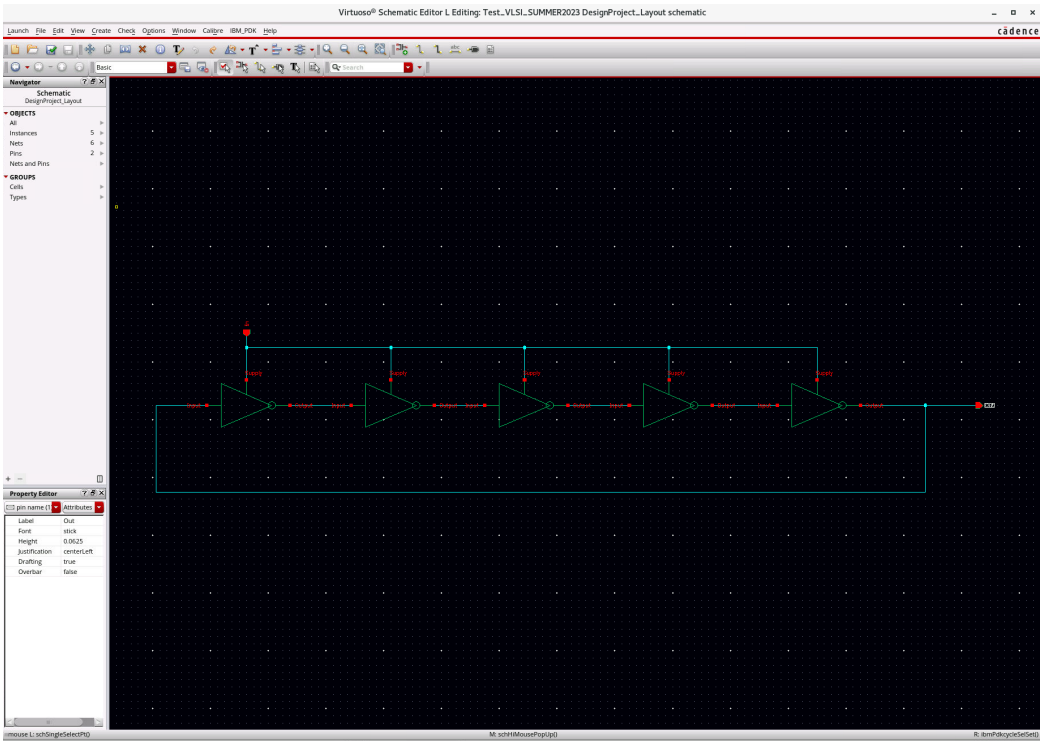

Figure 3: Represents the circuit the circuit schematic of the ring oscillator. After creating the schematic of the ring oscillator, I created a simulation test-bench to test the ring oscillator. The simulation test-bench is represented in Figure 4. I ran the simulation test-bench and got the results represented in Figure 5. From the results, I was able to compute the frequency of oscillation which is 1.06GHz. When it comes to the values, I used the following values: N = 5, Wn = 82um, Wp = 264um. I also use Vdd = 1.33V since it is less than 1.8V.

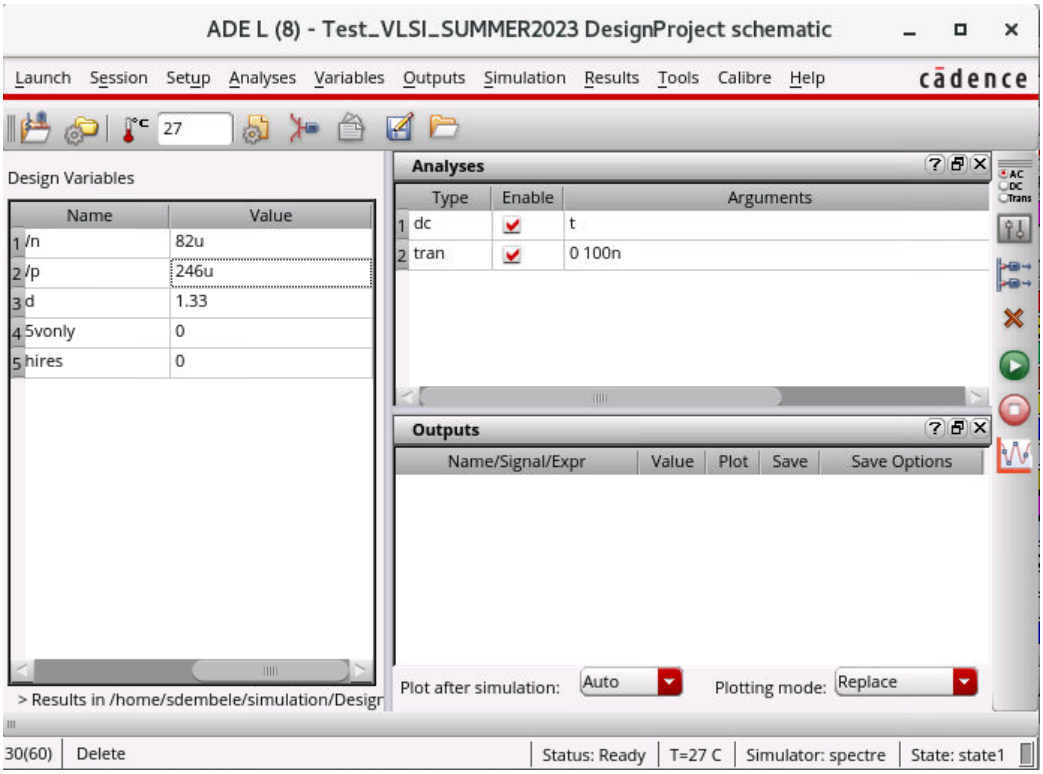

Figure 4: Represents the variables used for simulation of the ring oscillator.

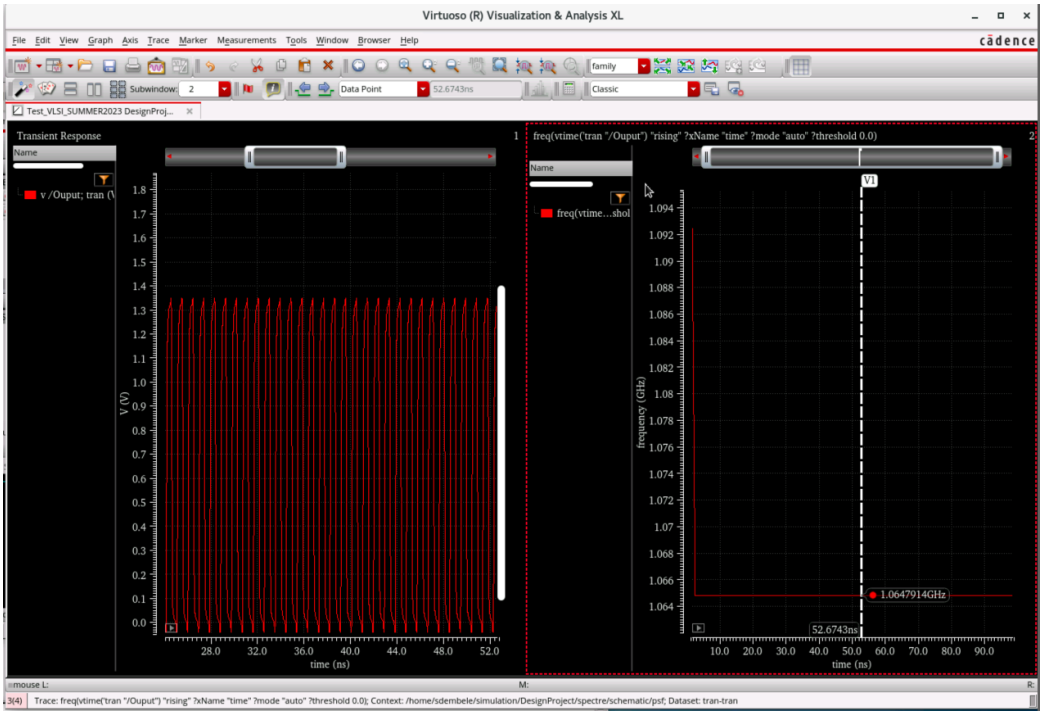

Figure 5: Represents the simulation results of the ring oscillator.

After plotting the simulation results, I was able to compute the frequency of oscillation which is 1.06GHz using calculator functionality from cadence the . When it comes to the values, I used the following values: N = 5, Wn = 82um, Wp = 264um, Vd = 1.33V.

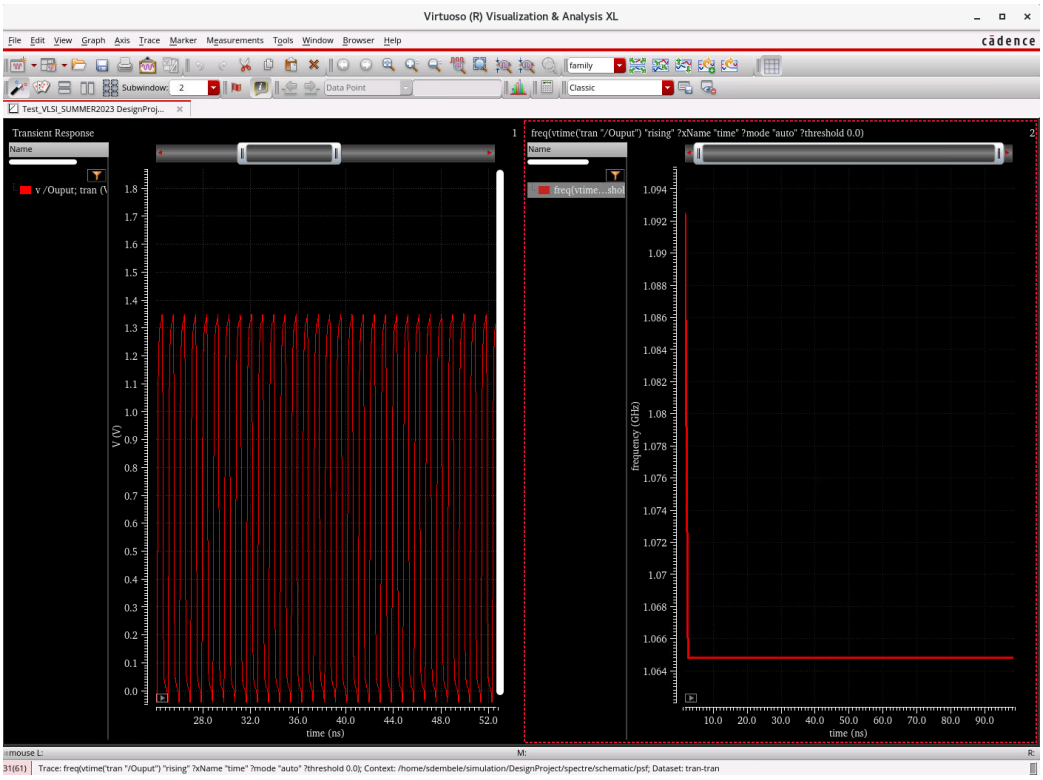

Figure 4: Represents the simulation test-bench of the ring oscillator.

Layout with DRC/LVS report

In this section I will show the layout of the ring oscillator and the DRC/LVS report. I started by creating a layout of a single inverter. Then I created a layout of the ring oscillator using the inverter layout. Finally, I ran the DRC/LVS report on the ring oscillator layout.

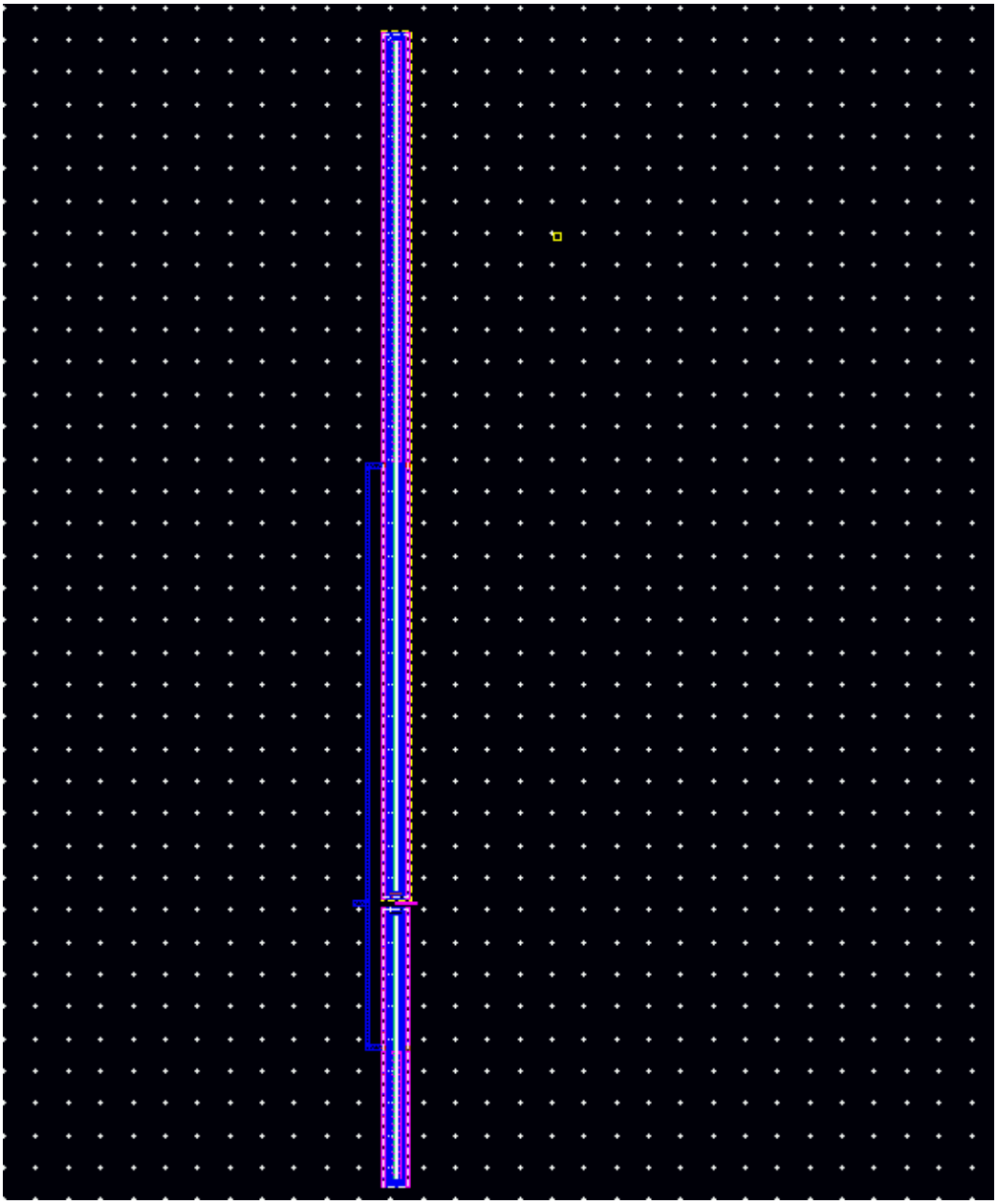

Figure 5: Represents the layout of a single inverter.

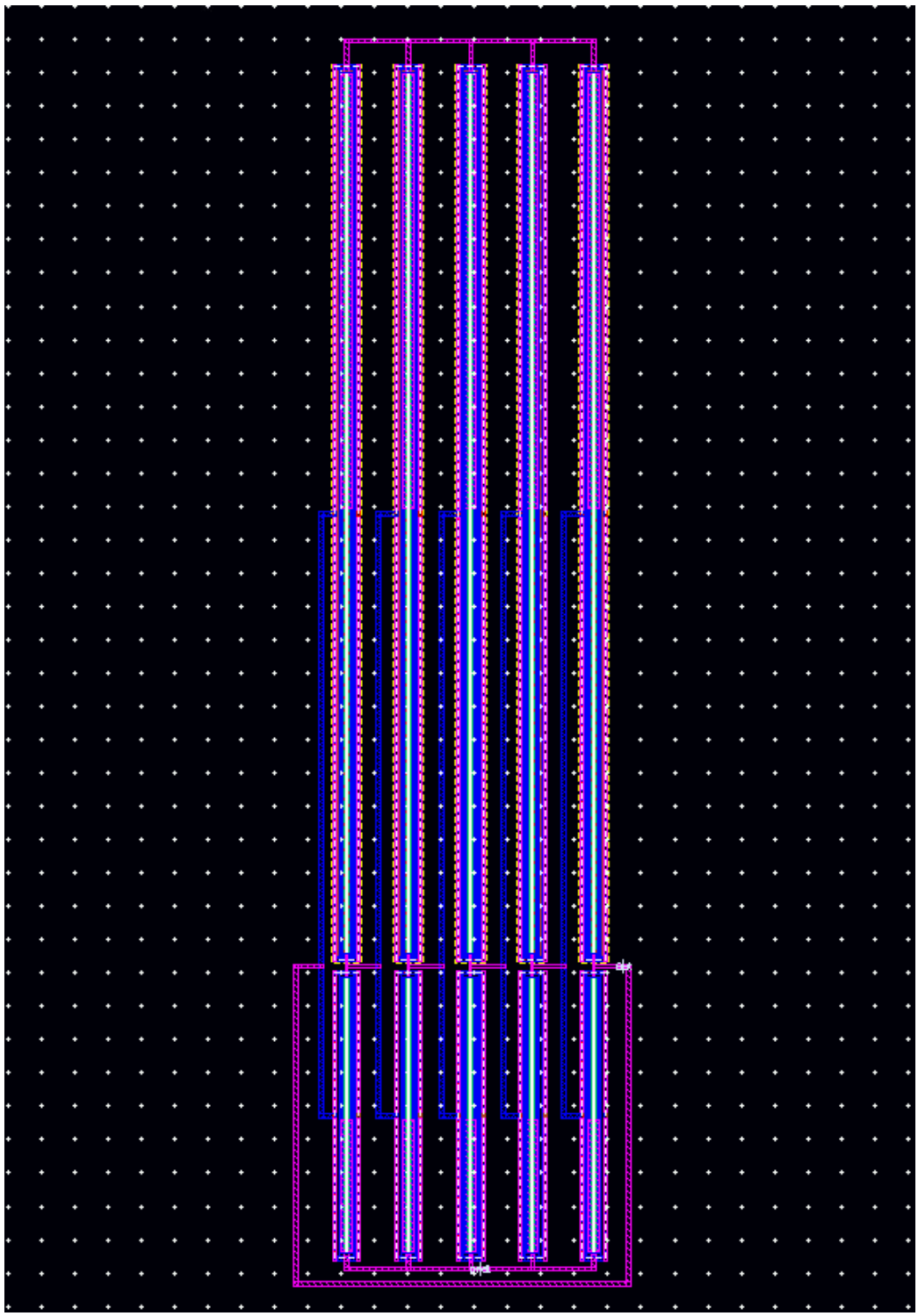

Figure 6: Represents the layout of the ring oscillator.

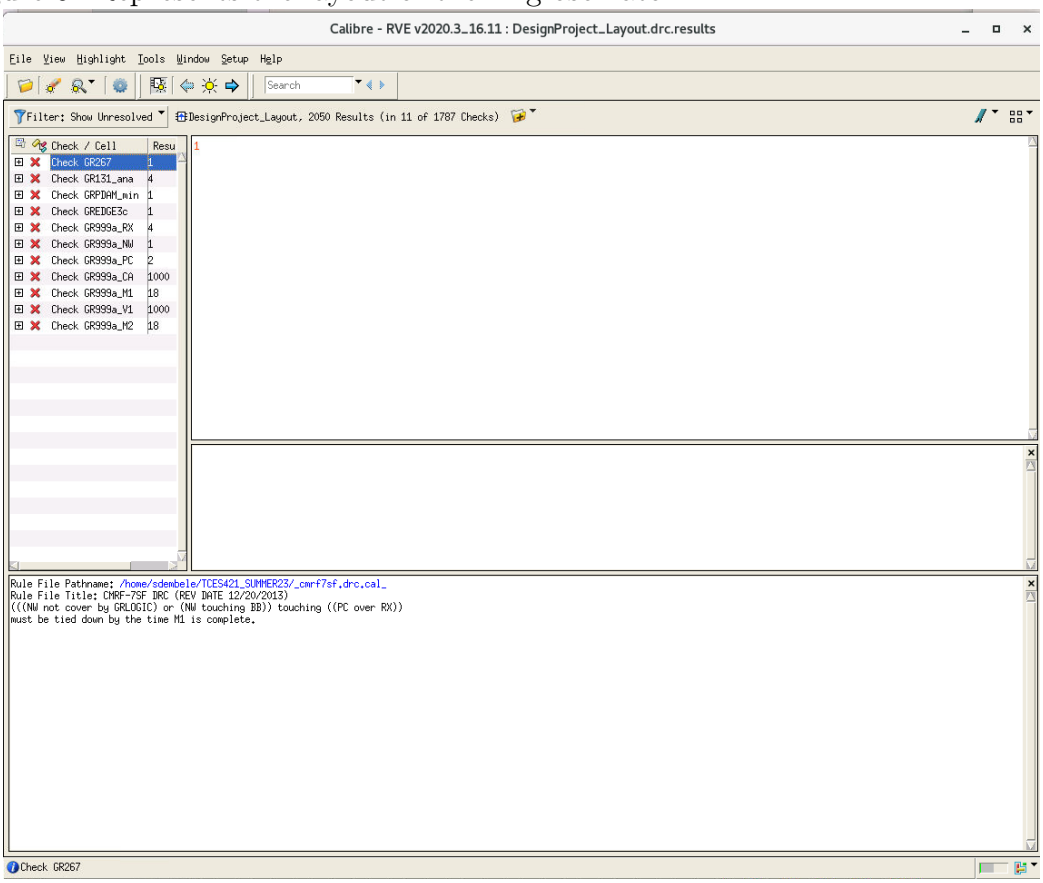

Figure 7: Represents the DRC report of the ring oscillator.

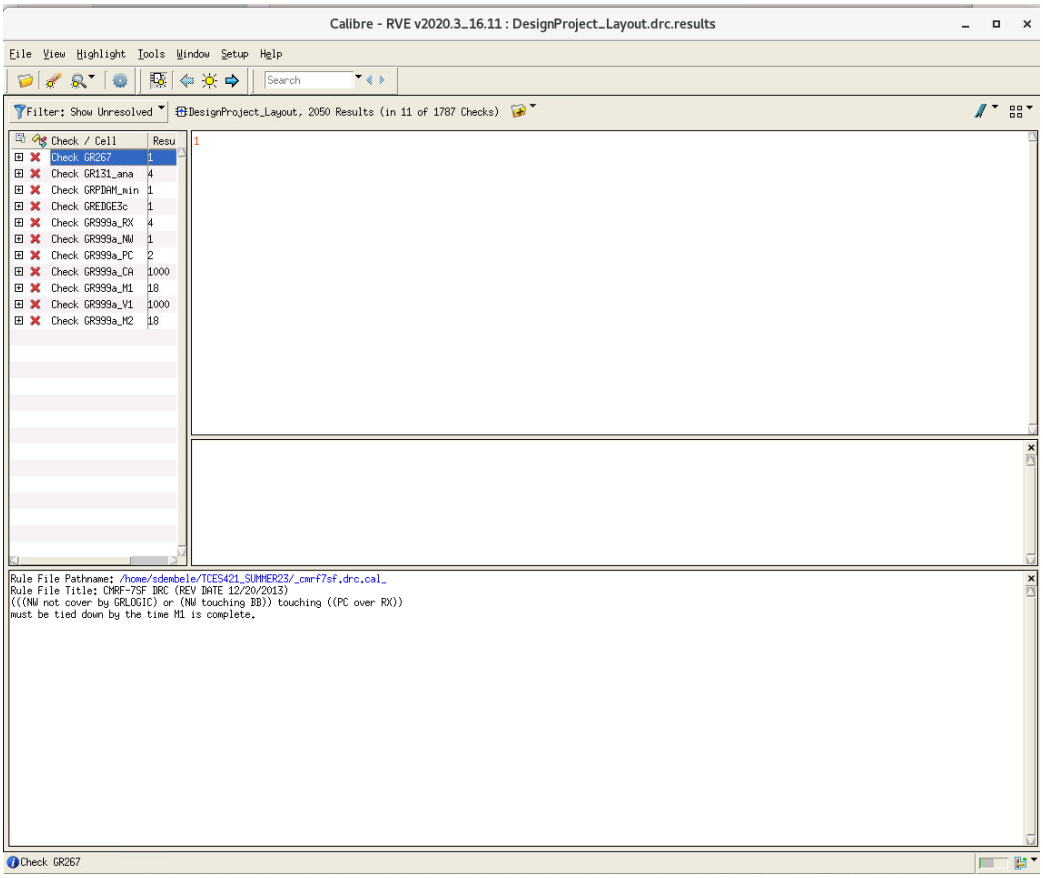

Figure 8: Represents the DRC report of the ring oscillator.

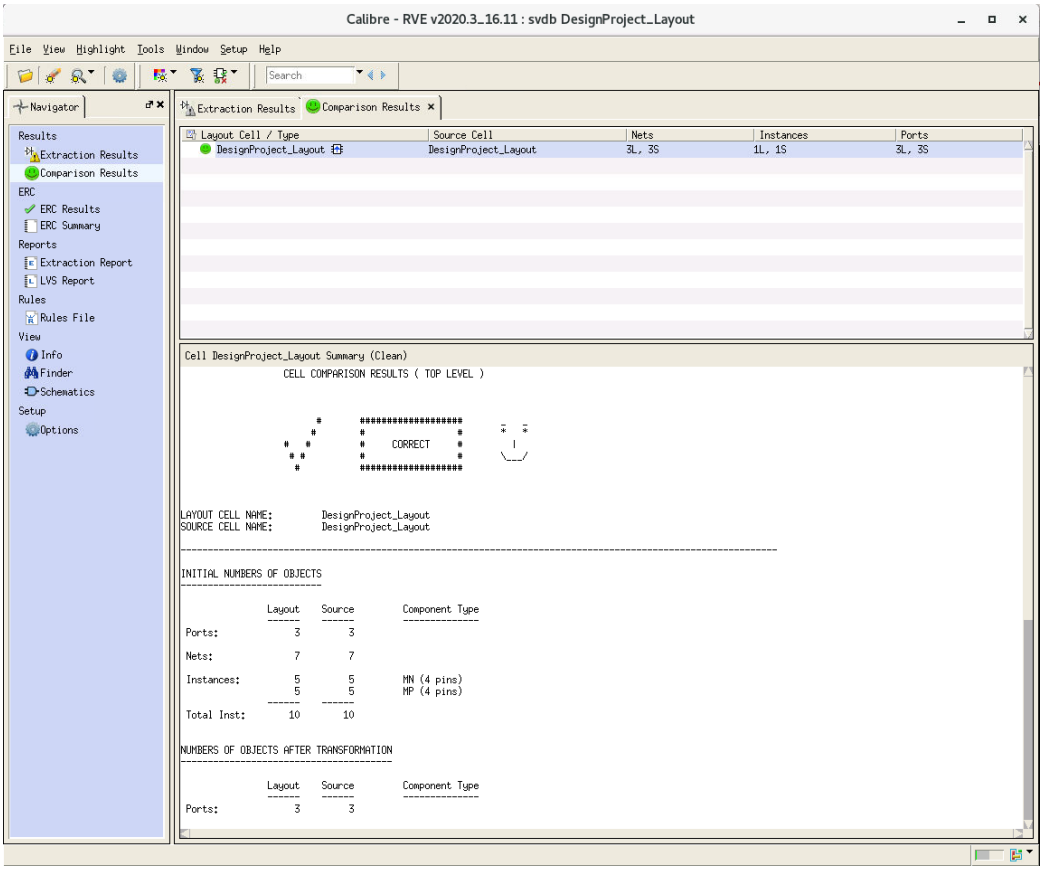

Figure 9: Represents the DRC report of the ring oscillator.

Summary

In conclusion, the goal of this project was to create a Ring Oscillator with specific design parameters and meet the frequency requirements while still being able to run a DRC/LVS report on the layout and use the IBM 0.18um CMOS process constraints. I was able to design the ring oscillator using the IBM 0.18um CMOS (cmrf7sf) process and all the requirements were met. In addition, I was able to run a DRC/LVS report on the layout and got no errors I used the IBM 0.18um CMOS process constraints and add the DRC/LVS report to the report. I face some minor issues at the beginning of the layout when the name of the pins was not matching, but using the debug messages

from cadence in LVS I was able to fix the issue and run a DRC/LVS report with no errors. Overall, this was a very great experience, I learned a lot from this project. I learned to optimize Ring Oscillator that operates at a specific frequency range. I learned how to design a ring oscillator using the IBM 0.18um CMOS (cmrf7sf) process. I also learned how to run a DRC/LVS report on a layout. I also learned how to use the calculator functionality from cadence to compute the frequency of oscillation of a ring oscillator. I also learned how to create a symbol from a schematic. I also learned how to create a simulation test bench. I also learned how to create a layout from a schematic. I also learned how to create a schematic from a layout. I also learned how to run a transient simulation o