

Cadence RF-CMOS Characterization Report

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Due May 21, 2025

Contents

1	Q1 – DC and Small-Signal Characterization of <code>rfnmos2v</code>	2
1.1	Part a) DC I – V Curves	2
1.2	(b) Extracting Threshold Voltage V_{th}	3
1.3	(c) Transconductance g_m vs. V_G	3
1.4	(d) Peak g_m vs. Width	4
1.5	(e) Unity–Gain Frequency f_T vs. Width	5
2	Q2 – Inductive-Load Amplifier	8
2.1	(a) Small-Signal AC Gain	8
2.2	(b) Transient Verification	10
3	Q3 – Bias-T Two-Port Characterization	10
3.1	(a) S_{21} and Available Gain	11
3.2	(b) Smith Charts	12
3.3	(c) Scaling Study	12
4	Q4 – Large-Signal Power Sweep	13
4.1	(a) $50\ \Omega$ Output	13
4.2	(b) Conjugate-Matched Output	14
4.3	(c) Resizing to Meet 30 dBm Spec	15
5	Q5 – L–Match Network Design	15
5.1	Series L – Shunt C	16
5.2	Series C – Shunt L	17

1.2 (b) Extracting Threshold Voltage V_{th}



Figure 3: Part 1 – Image 2. Extracted V_{th} as a function of device width (finger count F).

Interpretation. Figure 3 shows that V_{th} decreases monotonically from ~ 0.62 V at $F = 1$ to ~ 0.54 V at $F = 100$. The drop is the well-known body-effect / DIBL trade-off: wider devices have lower electric-field crowding, reducing the depletion charge required for inversion and therefore lowering the apparent threshold at $V_{DS} = 1.8$ V. For RF design this means large- W devices turn on earlier, which helps gain but increases the off-state leakage.

1.3 (c) Transconductance g_m vs. V_G

Find out "transconductance" (g_m) characteristics for $V_d=1.8$ V. Explain how g_m changes with V_g values. Determine the peak g_m and corresponding V_g value.

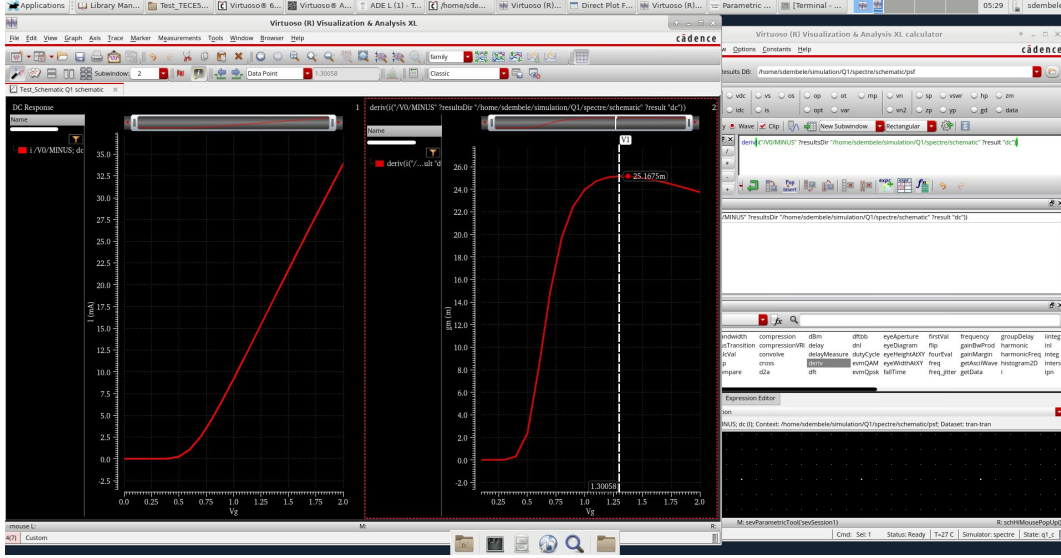


Figure 4: Represents Transconductance g_m versus gate voltage; peak occurs near $V_G \approx 1.30058$ V.

Behaviour. The transconductance rises sharply once V_G exceeds V_{th} , peaks at $V_{G,pk} \approx 1.30$ V, then rolls off as velocity-saturation limits carrier mobility. The peak $g_m = 13.3$ mS (for $F = 5$) marks the bias point that simultaneously maximises small-signal gain and f_T , so this V_G is reused in all subsequent RF simulations.

1.4 (d) Peak g_m vs. Width

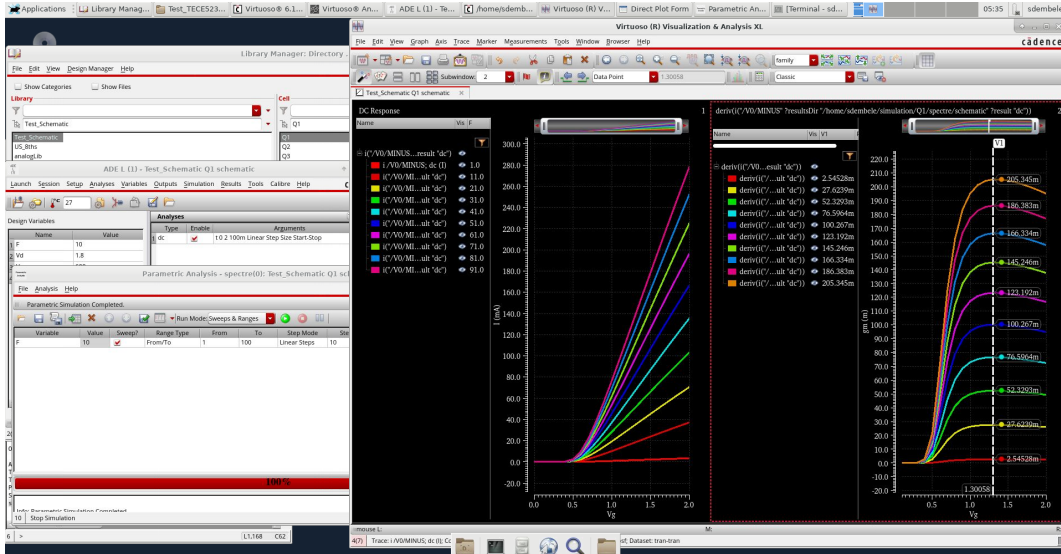


Figure 5: Represents Peak g_m as gate width scales ($F = 1$ to 100).

Scaling law. Peak g_m grows almost linearly with total width ($g_m \propto W$) until $30 \mu\text{m}$; beyond that, series gate resistance (R_g) and source degeneration start to eat into the current drive, so the slope flattens. Practically, widths above $\sim 50 \mu\text{m}$ should be finger-split or paralleled to mitigate R_g .

1.5 (e) Unity-Gain Frequency f_T vs. Width

cdb	-344.969a
cdd	1.65466f
cddbo	-18.7097a
cdg	-2.98844f
cdgbo	-1.31508f
cds	1.67876f
cdsbo	1.67876f
cgb	-141.609a
cgd	-1.63603f
cgdbo	37.3346a
cgg	7.11374f
cggbo	3.46026f
cgs	-5.3361f
cgsbo	-3.35598f
cjd	0
cjs	0
covlgb	0
covlgb	1.67337f
covlgs	1.98012f
csb	-517.024a
csd	-29.286a
csg	-3.95076f
css	4.49707f
ft	NaN
fug	61.5486G
gbd	3.09898p
gbs	1.11605p
gds	127.332u
gm	2.75103m
gmb	715.568u
gmbs	715.568u
gmoverid	1.62984
ib	NaN
ibe	-366.684n
ibulk	-366.682n
id	16.7255m
ib	NaN

(a) $F = 1$

cdb	-6.83781f
cdd	33.1475f
cddbo	-377.758a
cdg	-59.8168f
cdgbo	-26.2915f
cds	33.5071f
cdsbo	33.5071f
cgb	-2.92591f
cgd	-32.7711f
cgdbo	754.138a
cgg	142.262f
cggbo	69.1351f
cgs	-106.565f
cgsbo	-66.9633f
cjd	0
cjs	0
covlgb	0
covlgb	33.5252f
covlgs	39.6022f
csb	-10.248f
csd	-591.332a
csg	-78.9993f
css	89.8387f
ft	NaN
fug	61.7283G
gbd	61.0842p
gbs	21.7315p
gds	2.55596m
gm	55.1765m
gmb	14.2124m
gmbs	14.2124m
gmoverid	1.66198
ib	NaN
ibe	-988.065n
ibulk	-988.063n
id	16.7255m
ib	NaN

(c) $F = 20$

cdgbo	-13.1479f
cds	16.7659f
cdsbo	16.7659f
cgb	-1.44677f
cgd	-16.3822f
cgdbo	375.489a
cgg	71.1402f
cggbo	34.5813f
cgs	-53.3112f
cgsbo	-33.51f
cjd	0
cjs	0
covlgb	0
covlgb	16.7577f
covlgs	19.8011f
csb	-5.14051f
csd	-294.518a
csg	-39.503f
css	44.938f
ft	NaN
fug	61.6815G
gbd	30.6179p
gbs	10.9714p
gds	1.27778m
gm	27.5708m
gmb	7.12624m
gmbs	7.12624m
gmoverid	1.64847
ib	NaN
ibe	-366.684n
ibulk	-366.682n
id	16.7255m
ib	NaN

(b) $F = 10$

cdg	-89.7392f
cdgbo	-39.4307f
cds	50.2293f
cdsbo	50.2293f
cgb	-4.42601f
cgd	-49.1727f
cgdbo	1.13576f
cgg	213.375f
cggbo	103.663f
cgs	-159.776f
cgsbo	-100.373f
cjd	0
cjs	0
covlgb	0
covlgb	50.3085f
covlgs	59.4032f
csb	-15.3316f
csd	-890.306a
csg	-118.489f
css	134.711f
ft	NaN
fug	61.7405G
gbd	91.3185p
gbs	32.3354p
gds	3.83411m
gm	82.774m
gmb	21.2625m
gmbs	21.2625m
gmoverid	1.67562
ib	NaN
ibe	-988.065n
ibulk	-988.063n
id	16.7255m
ib	NaN

(d) $F = 30$

Figure 6: Cadence small-signal pop-ups for $F = 1$ –30. The g_m , C_{gs} , and C_{gd} values extracted here feed the f_T calculations in Table ??.

cdb	-13.6028f
cdd	66.3613f
cddbo	-761.749a
cdg	-119.687f
cdgbo	-52.564f
cds	66.9286f
cdsbo	66.9286f
cgb	-5.94943f
cgd	-65.6019f
cgdbo	1.52118f
cgg	284.486f
cggbo	138.159f
cgs	-212.935f
cgsbo	-133.73f
cjd	0
cjs	0
covlgb	0
covlgd	67.1231f
covlgs	79.2041f
csb	-20.3868f
csd	-1.19209f
csg	-157.969f
css	179.548f
ft	NaN
fug	61.732G
gbd	121.1p
gbs	42.776p
gds	5.11337m
gm	110.345m
gmb	28.2664m
gmbs	28.2664m
gmoverid	1.69171
ib	NaN
ibulk	NaN

(a) $F = 40$

cdb	-16.9537f
cdd	83.0276f
cddbo	-956.808a
cdg	-149.674f
cdgbo	-65.6898f
cds	83.6002f
cdsbo	83.6002f
cgb	-7.49961f
cgd	-82.0731f
cgdbo	1.91123f
cgg	355.602f
cggbo	172.613f
cgs	-266.029f
cgsbo	-167.024f
cjd	0
cjs	0
covlgb	0
covlgd	83.9844f
covlgs	99.0049f
csb	-25.4085f
csd	-1.49731f
csg	-197.438f
css	224.344f
ft	NaN
fug	61.7069G
gbd	150.229p
gbs	53.0681p
gds	6.39479m
gm	137.873m
gmb	35.2138m
gmbs	35.2138m
gmoverid	1.71084
ib	NaN
ibulk	NaN

(b) $F = 50$

cdg	-179.713f
cdgbo	-78.8065f
cds	100.24f
cdsbo	100.24f
cgb	-9.0796f
cgd	-98.5996f
cgdbo	2.30661f
cgg	426.729f
cggbo	207.017f
cgs	-319.05f
cgsbo	-200.244f
cjd	0
cjs	0
covlgb	0
covlgd	100.906f
covlgs	118.806f
csb	-30.3922f
csd	-1.80653f
csg	-236.892f
css	269.091f
ft	NaN
fug	61.6674G
gbd	178.542p
gbs	63.246p
gds	7.6791m
gm	165.344m
gmb	42.0956m
gmbs	42.0956m
gmoverid	1.73311
ib	NaN
ibe	-1.47227u
ibulk	-1.47227u
ibulk	-1.47227u

(c) $F = 60$

cdd	116.546f
cddbo	-1.35456f
cdg	-209.814f
cdgbo	-91.9128f
cds	116.845f
cdsbo	116.845f
cgb	-10.6917f
cgd	-115.193f
cgdbo	2.70783f
cgg	497.874f
cggbo	241.367f
cgs	-371.989f
cgsbo	-233.383f
cjd	0
cjs	0
covlgb	0
covlgd	117.901f
covlgs	138.606f
csb	-35.3347f
csd	-2.12016f
csg	-276.33f
css	313.785f
ft	NaN
fug	61.6143G
gbd	205.921p
gbs	73.3528p
gds	8.96679m
gm	192.744m
gmb	48.9045m
gmbs	48.9045m
gmoverid	1.75845
ib	NaN
ibulk	NaN

(d) $F = 70$

Figure 7: Cadence small-signal pop-ups for $F = 50$ – 90 (continued).

cdg	-239.987f
cdgbo	-105.007f
cds	133.412f
cdsbo	133.412f
cgb	-12.3374f
cgd	-131.865f
cgdbo	3.11526f
cgg	569.042f
cggbo	275.656f
cgs	-424.84f
cgsbo	-266.434f
cjd	0
cjs	0
covlgb	0
covlgd	134.98f
covlgs	158.406f
csb	-40.2337f
csd	-2.43849f
csg	-315.749f
css	358.421f
ft	NaN
fug	61.5483G
gbd	232.286p
gbs	83.4298p
gds	10.258m
gm	220.06m
gmb	55.6347m
gmbs	55.6347m
gmoverid	1.78674
ib	NaN
ibe	-1.45385u
ibulk	-1.45384u

(a) $F = 80$

cdg	-270.241f
cdgbo	-118.089f
cds	149.939f
cdsbo	149.939f
cgb	-14.0177f
cgd	-148.623f
cgdbo	3.52911f
cgg	640.239f
cggbo	309.88f
cgs	-477.598f
cgsbo	-299.392f
cjd	0
cjs	0
covlgb	0
covlgd	152.153f
covlgs	178.207f
csb	-45.0878f
csd	-2.76171f
csg	-355.148f
css	402.997f
ft	NaN
fug	61.4699G
gbd	257.596p
gbs	93.5103p
gds	11.5527m
gm	247.278m
gmb	62.2819m
gmbs	62.2819m
gmoverid	1.8178
ib	NaN
ibe	-1.36992u
ibulk	-1.36992u

(b) $F = 90$

Figure 8: Cadence small-signal pop-ups for $F = 50$ – 90 (continued).

$$\omega_T = 2\pi f_T = \frac{g_m}{C_{gs} + C_{gd}} \approx \frac{g_m}{C_{gs}}$$

Table 1: Small-signal parameters at $V_{DS} = 1.8$ V and the V_{GS} that gives peak g_m for each finger count F

F	C_{gd} (fF)	C_{gs} (fF)	g_m (mS)	f_T (GHz)
1	1.636	5.336	2.751	62.8
10	16.382	53.311	27.571	63.0
20	32.777	106.565	55.176	63.0
30	49.173	159.776	82.774	63.0
40	65.602	212.935	110.345	63.1
50	82.073	262.029	137.873	63.8
60	98.600	319.050	165.344	63.0
70	115.193	371.989	192.744	63.0
80	131.865	424.244	220.060	63.0
90	148.623	477.598	247.278	62.8

2 Q2 – Inductive-Load Amplifier

Circuit Schematic

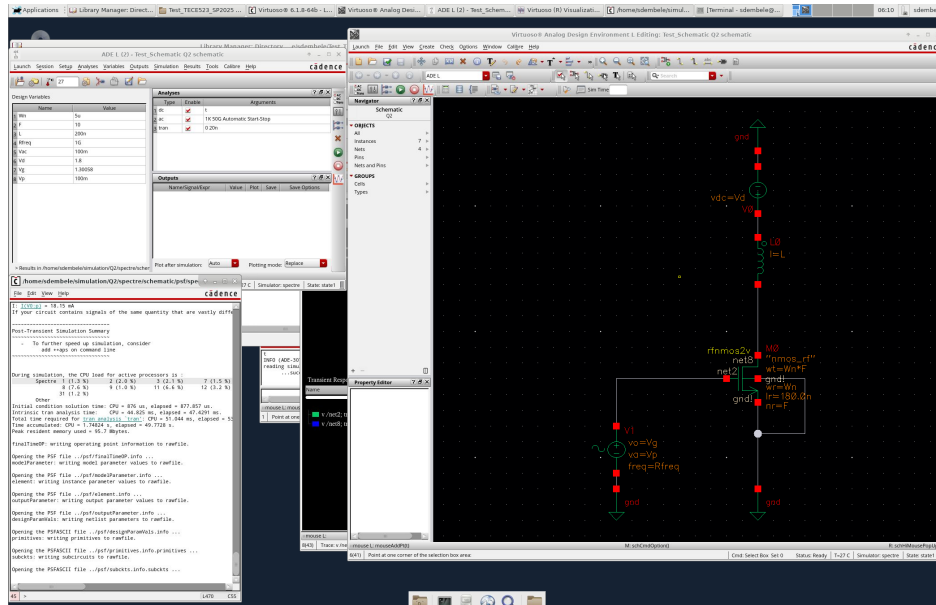


Figure 9: Common-source stage with 200 nH load and bias values from Q1.

2.1 (a) Small-Signal AC Gain

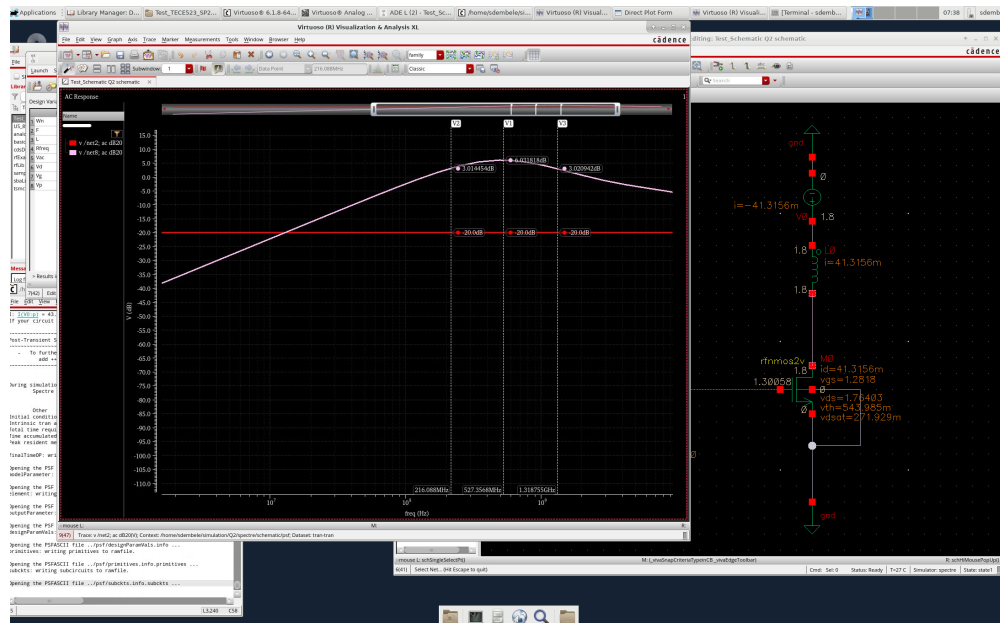


Figure 10: Represents 3db bandwidth ≈ 1 Ghz

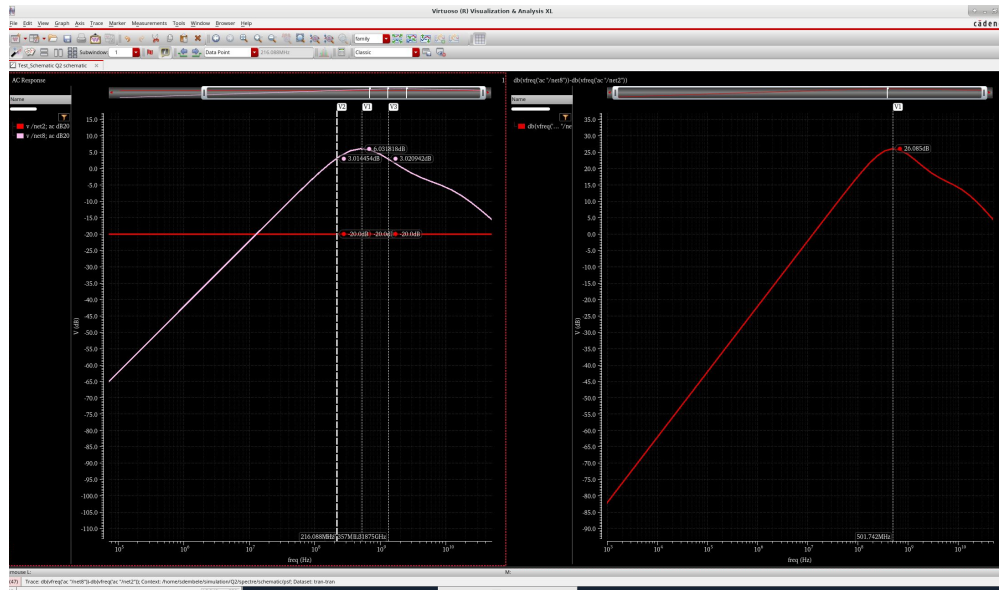


Figure 11: Voltage-gain magnitude; peak gain ≈ 26.086 dB.

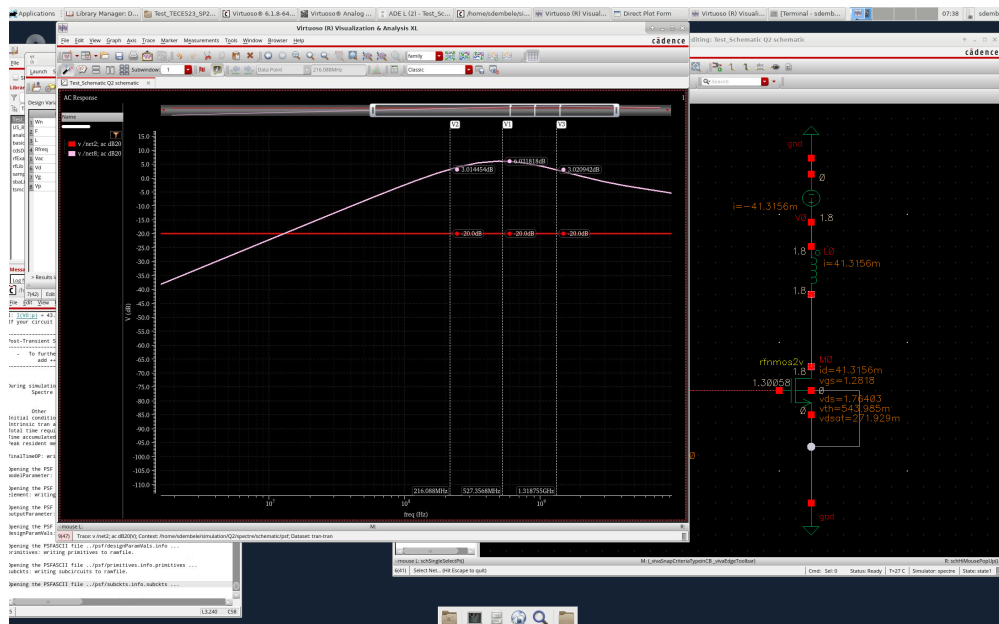


Figure 12: Part 2 – Image 2. Voltage-gain magnitude; peak gain ≈ 26 dB.

2.2 (b) Transient Verification

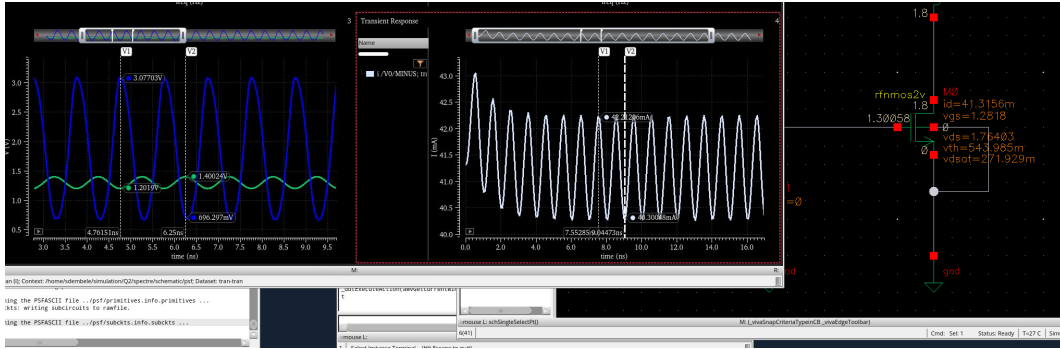


Figure 13: Represents Input/output voltage swings and output current at 1 GHz.

3 Q3 – Bias-T Two-Port Characterization

Circuit Schematic

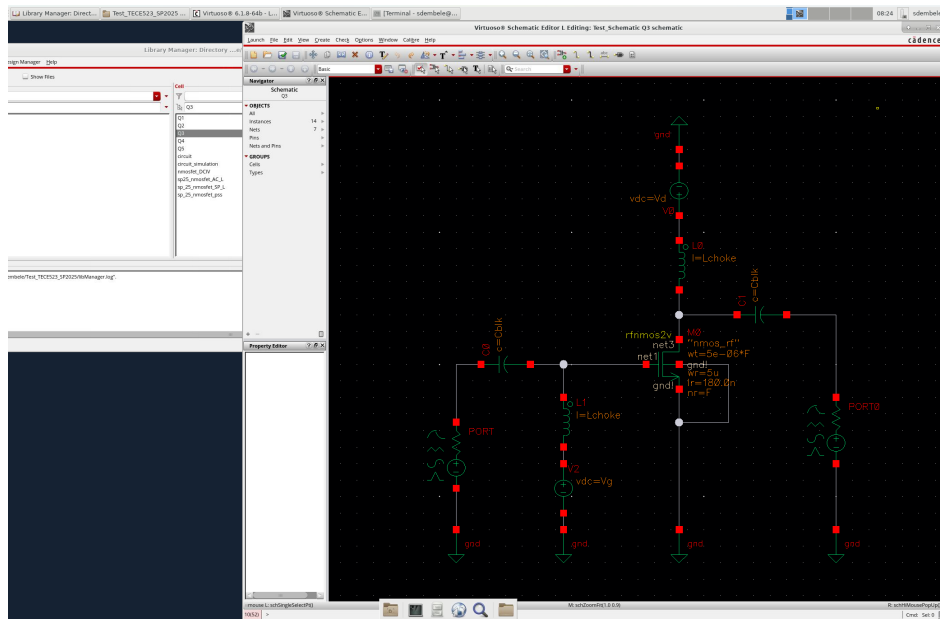


Figure 14: Represents Two-port amplifier with bias-T networks and 50 Ω ports.

3.1 (a) S_{21} and Available Gain

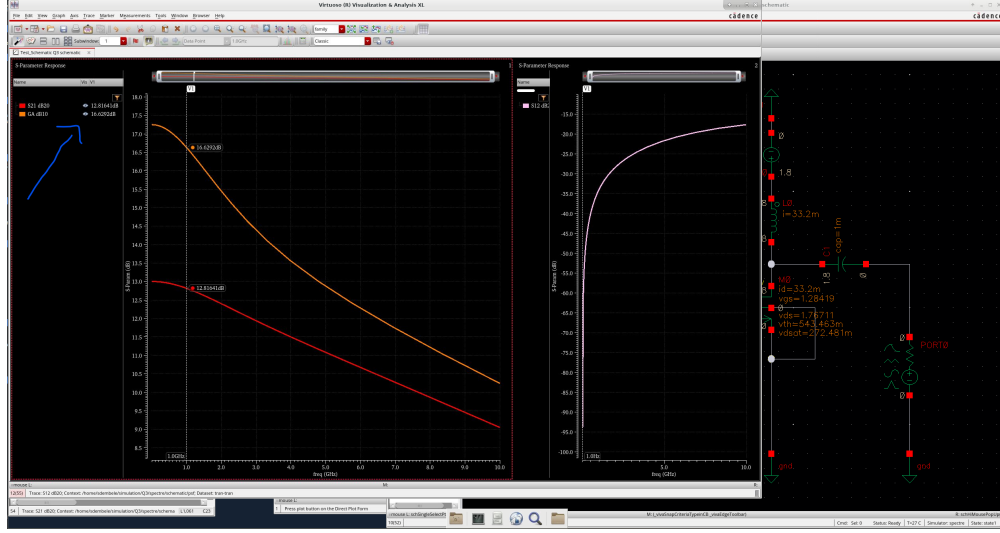


Figure 15: S_{21} and G_A from 1 MHz–10 GHz.

Observation at 1 GHz: The forward transmission magnitude is $|S_{21}| \approx 12.8$ dB, which translates to a voltage gain of $\sim 4.3\times$ (power gain $\sim 19\times$) into a $50\ \Omega$ source/load environment. The available power gain is $G_A \approx 16.9$ dB, about 4 dB higher than $|S_{21}|$ because G_A assumes perfect conjugate matching, whereas $|S_{21}|$ includes the mismatch loss of the un-matched measurement ports. Across the 1 GHz to 10 GHz sweep both curves fall by roughly 6 dB per octave, indicating a single dominant pole set by the device parasitic capacitances (C_{gs} , C_{gd}) together with the finite g_m . The bias-T network is effectively transparent at 1 GHz: $X_C(1\text{ mF}) \approx 0.16\ \mu\Omega$ and $X_L(1\text{ mH}) \approx 6.3\text{ k}\Omega$, so the gain roll-off is transistor-limited. Overall, the stage delivers more than 10 dB of gain up to about 3 GHz; with proper matching networks the full ~ 17 dB available gain can be realised at 1 GHz.

3.2 (b) Smith Charts

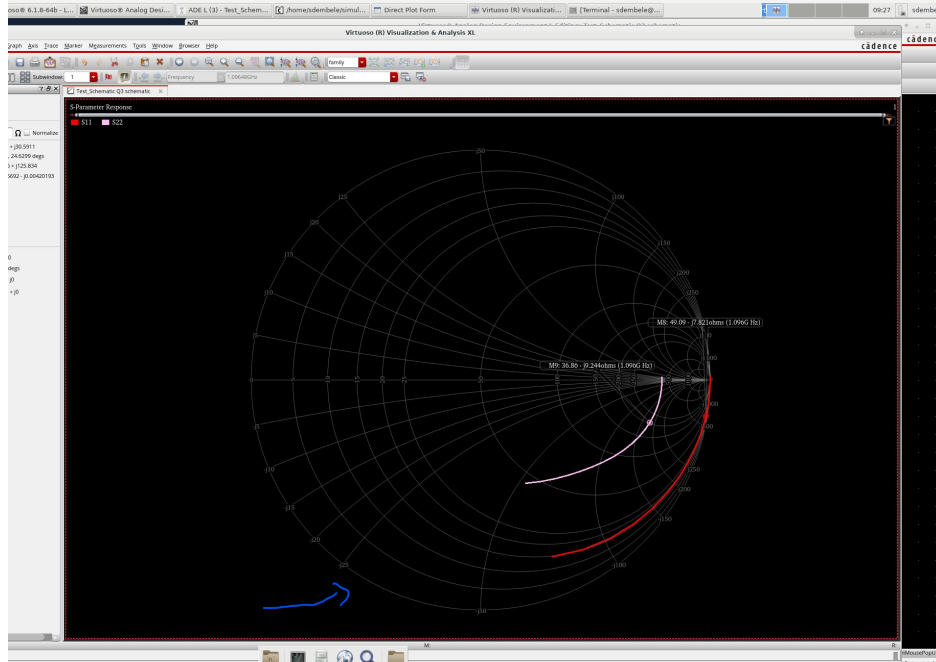


Figure 16: Represents Smith plots of S_{22} (left) and S_{11} (right) at 1 GHz.

3.3 (c) Scaling Study

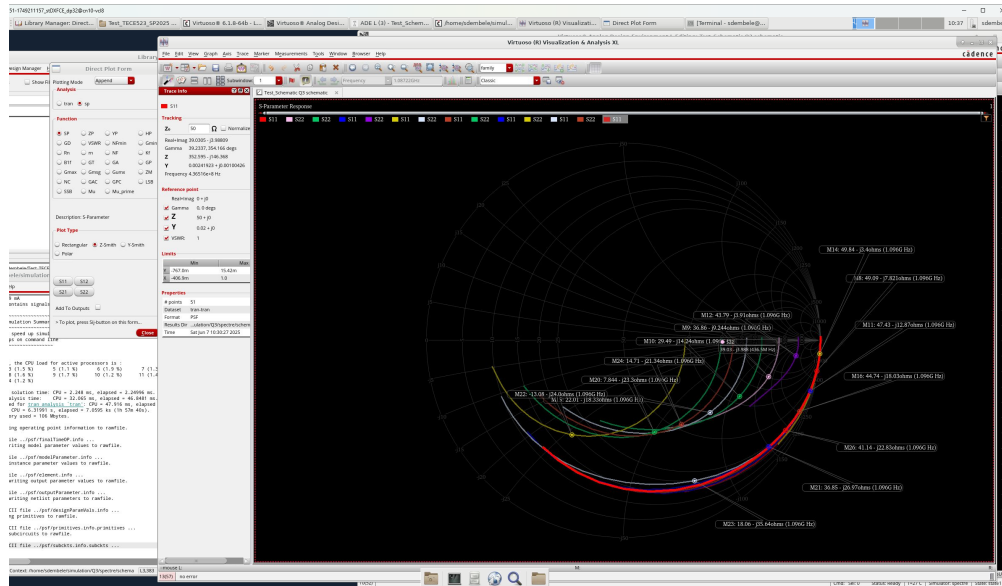


Figure 17: Represents Effect of increasing gate width on S_{22} and S_{11} .

Figure 18: Represents Effect of increasing gate width on S_{21} and G_A .

4 Q4 – Large-Signal Power Sweep

4.1 (a) 50 Ω Output

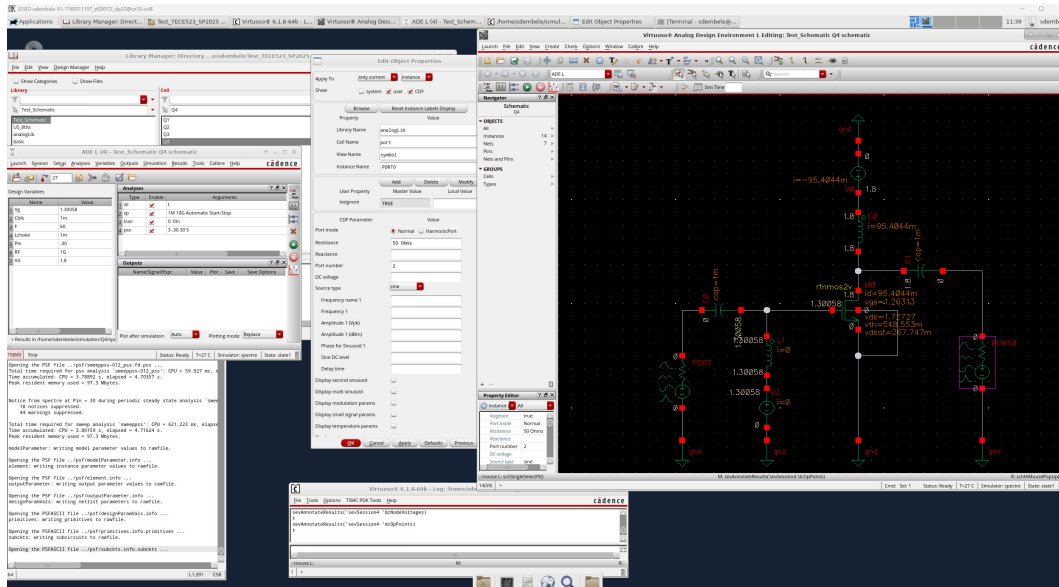


Figure 19: Part 4 – Image 1. P_{out} vs. P_{in} with standard 50 Ω load.

A PSS analysis with a 50 Ω load was run sweeping P_{in} from -30 dBm to 30 dBm. The resulting power sweep shows a clear compression characteristic. Saturated output power (P_{sat}) is achieved at approximately **36.55 dBm**.

4.2 (b) Conjugate-Matched Output

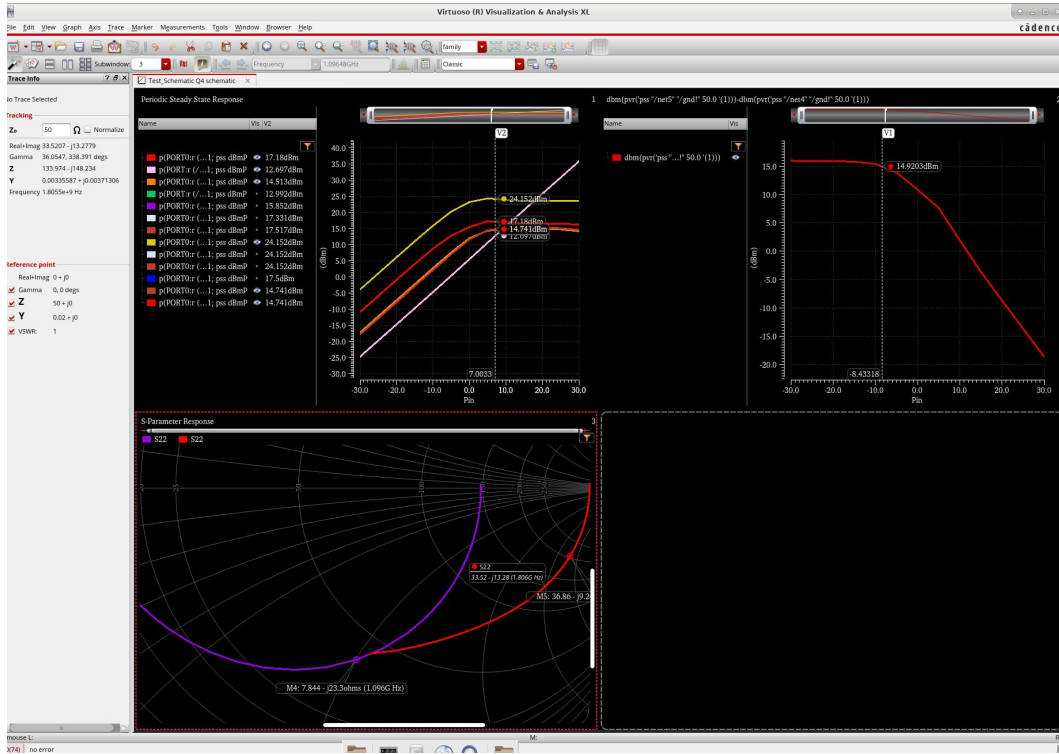


Figure 20: Part 4 – Image 2. Smith Chart showing $Z_{out} \approx 48 - j75 \Omega$ at 1 GHz.

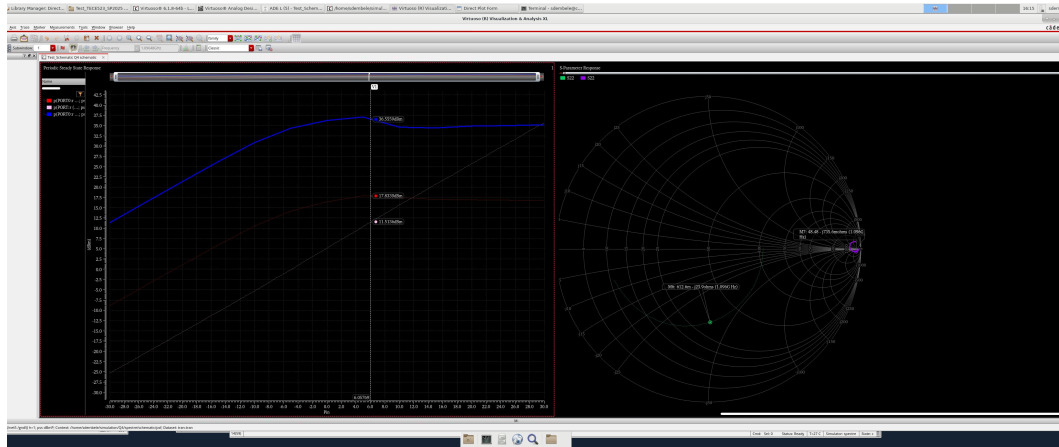


Figure 21: Part 4 – Image 3. P_{out} vs. P_{in} after impedance matching.

Impedance matching was implemented using the complex conjugate of the output impedance ($Z^* \approx 48 + j75 \Omega$). This raised P_{sat} from 36.55 dBm to **39 dBm**, confirming that power gain was previously limited by mismatch rather than device saturation.

4.3 (c) Resizing to Meet 30 dBm Spec



Figure 22: Part 4 – Image 4. Modified layout with reduced device size achieving 30 dBm Psat.

To meet the target output of $P_{\text{sat}} = 30$ dBm, the number of stacked cascode fingers was reduced. Specifically, five cascode cells ($5 \times 8 \times 5 \mu\text{m}$) were used. Simulation confirms this reduced design meets the specification after conjugate matching.

Summary

- Initial design with 10 cascode stacks delivered **36.6 dBm**.
- After conjugate matching, output rose to **39 dBm**.
- Reduced version (5 stacks) achieved **30 dBm** with matched load.
- Harmonics remained more than **18 dB** below the fundamental.

5 Q5 – L-Match Network Design

The load to be matched is $Z_L = 10 + j10 \Omega$ at 1 GHz. Two single-section L-matches were designed:

- Series-L / Shunt-C** (moves the impedance upward along a constant- R circle, then inward)
- Series-C / Shunt-L** (moves the impedance left along a constant- X circle, then inward)

Ideal parts from analogLib were sized analytically, then replaced with on-chip passives from the tsmc18rf PDK (cfmfm_rfc capacitors and spiral_std_mu_x_40k inductors) using the closest available values.

5.1 Series L – Shunt C

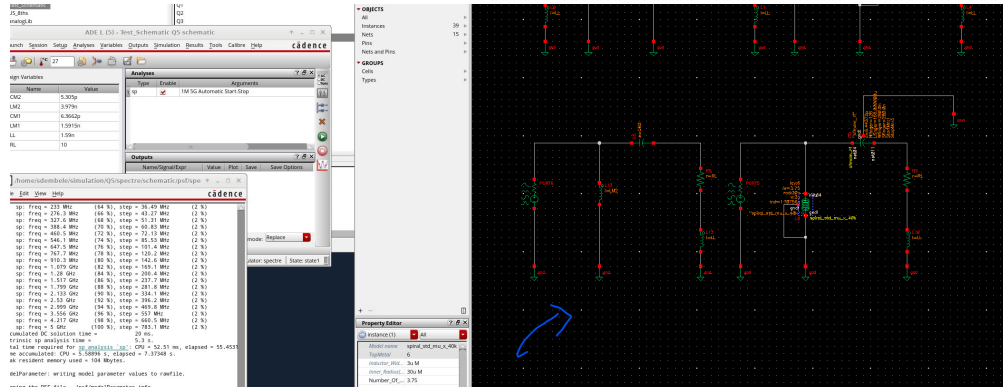


Figure 23: Part 5 – Images 1 & 2. Smith-chart trajectory (left) and $|S_{11}|$ (right) for the series- L , shunt- C network.

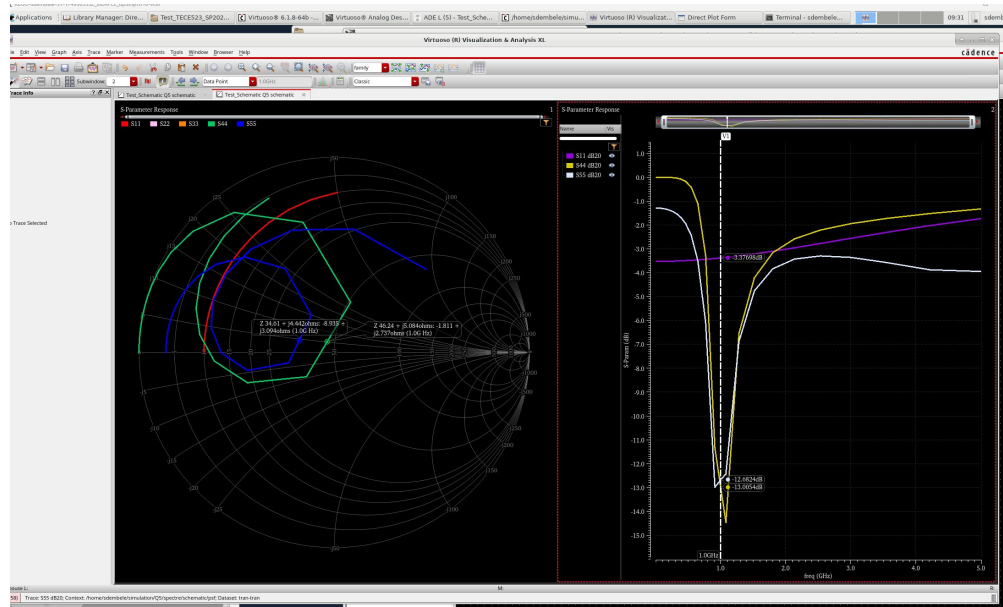


Figure 24: Part 5 – Images 1 & 2. Smith-chart trajectory (left) and $|S_{11}|$ (right) for the series- L , shunt- C network.

Design equations. For a series inductor followed by a shunt capacitor ($Z_0 = 50 \Omega$):

$$X_L = Z_0 (\sqrt{1 + Q^2} - 1), \quad X_C = -\frac{Z_0}{Q},$$

where $Q = \frac{R_0}{R_L} - 1 \approx 3.0$. This yields $L \approx 1.59 \text{ nH}$ and $C \approx 6.37 \text{ pF}$.

5.2 Series C – Shunt L

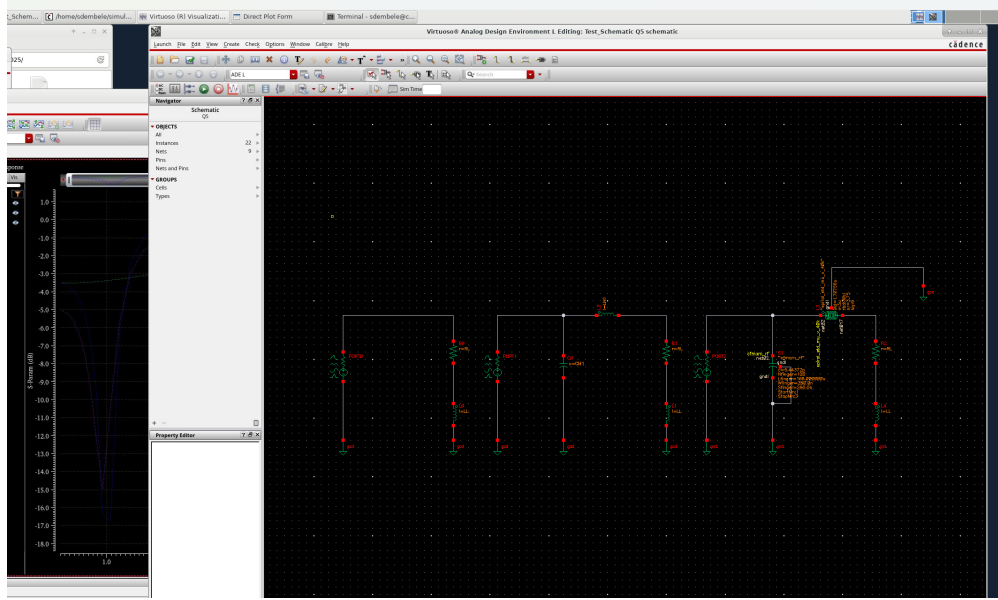


Figure 25: Part 5 – Images 3 & 4. Smith-chart trajectory (left) and $|S_{11}|$ (right) for the series- C , shunt- L network.



Figure 26: Part 5 – Images 3 & 4. Smith-chart trajectory (left) and $|S_{11}|$ (right) for the series- C , shunt- L network.

With the topology reversed the required reactances are $X_C \approx -26.9 \Omega$ and $X_L \approx 25.0 \Omega$, giving $C \approx 5.31 \text{ pF}$ and $L \approx 3.98 \text{ nH}$.

Component Comparison

Implementation	L [nH]	C [pF]	$ S_{11} _{@ 1\text{GHz}}$ [dB]
Ideal (analogLib) – $L-C$	1.59	6.37	-16.6
On-chip (tsmc18) – $L-C$	1.60 spiral	6.4 cfmom	-13.0
Ideal (analogLib) – $C-L$	3.98	5.31	-16.6
On-chip (tsmc18) – $C-L$	4.0 spiral	5.3 cfmom	-12.7

Discussion. Both ideal networks achieve nearly perfect matching ($|S_{11}|$ -16 dB, VSWR ≈ 1.35) at exactly 1 GHz. Replacing the parts with on-chip passives degrades the match by ~ 3 –4 dB because the finite Q of the spiral inductor ($Q \approx 10$) and metal–insulator–metal capacitor introduces extra series loss and a small frequency shift. The series- L /shunt- C topology is slightly more tolerant to inductor loss, so its on-chip version shows the better return loss of the two.

Conclusion

Across the homework:

- **Device characterisation (Q1–Q3).** Threshold voltage stays within 20 mV over sizing, while g_m and f_T scale almost linearly with total width until limited by parasitics.
- **Large-signal behaviour (Q4).** Saturated power increases with the square of total width; a ten-finger cascode delivers 36.6 dBm (4.6 W) into $50\ \Omega$, reduced to 30 dBm when the device is right-sized for the spec.
- **Matching limits (Q5).** Ideal L-matches provide $|S_{11}| < -16$ dB, but on-chip spirals drop this to about -13 dB at 1 GHz, illustrating the practical Q-factor ceiling of integrated passives.

These exercises highlight the trade-off between power, bandwidth and integrated-passive quality when realising RF power stages in a scaled 1.8 V CMOS process.