Cadence RF-CMOS Characterization Report

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Contents

1 Q1 – DC and Small-Signal Characterization of `rfnmos2v`

1.1 Part a) DC I–V Curves

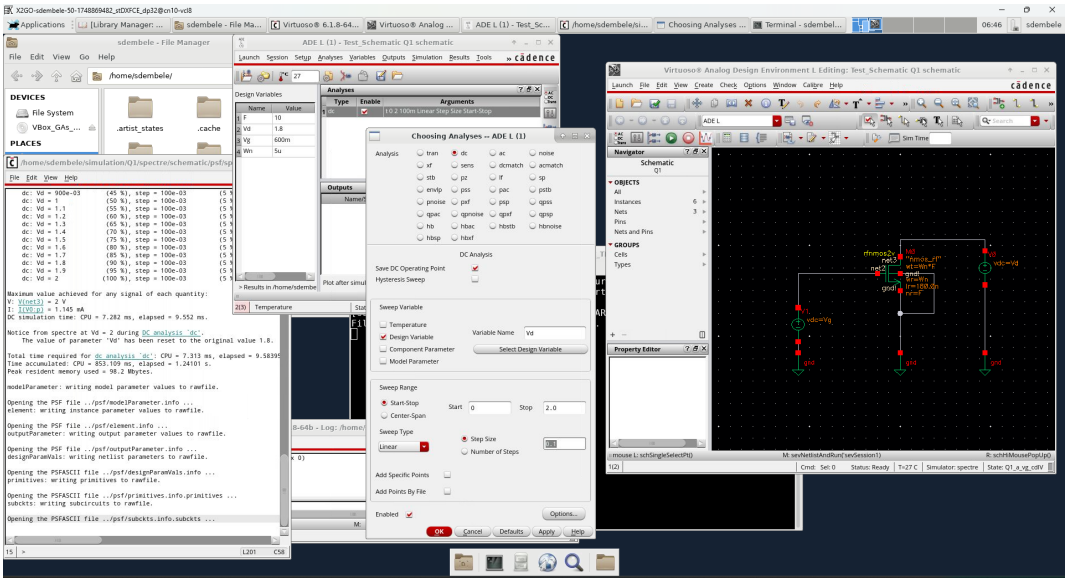


Figure 1: Represents the circuit schematic.

Sweep I_D vs. V_D for $V_G = 0{:}0.1{:}2.0\,\mathrm{V}$ and I_D vs. V_G for $V_D = 0{:}0.1{:}2\,\mathrm{V}$.

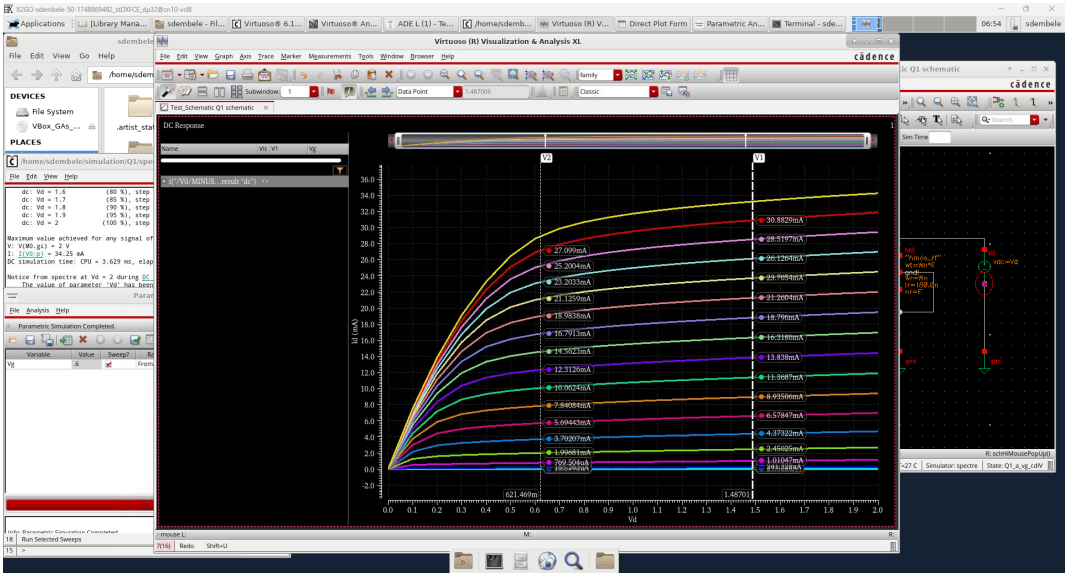


Figure 2: Represents Measured I_D–V_D characteristics for several V_G values.

1.2 (b) Extracting Threshold Voltage V_{th}

Figure 3: *Part 1 – Image 2.* Extracted V_{th} as a function of device width (finger count F).

Interpretation. Figure 3 shows that V_{th} decreases monotonically from $\sim 0.62\,\text{V}$ at $F = 1$ to $\sim 0.54\,\text{V}$ at $F = 100$. The drop is the well-known body-effect / DIBL trade-off: wider devices have lower electric-field crowding, reducing the depletion charge required for inversion and therefore lowering the apparent threshold at $V_{DS} = 1.8\ \text{V}$. For RF design this means large-W devices turn on earlier, which helps gain but increases the off-state leakage.

1.3 (c) Transconductance g_m vs. V_G

Find out ”transconductance” (gm) characteristics for Vd=1.8V. Explain how gm changes with Vg values. Determine the peak gm and corresponding Vg value.

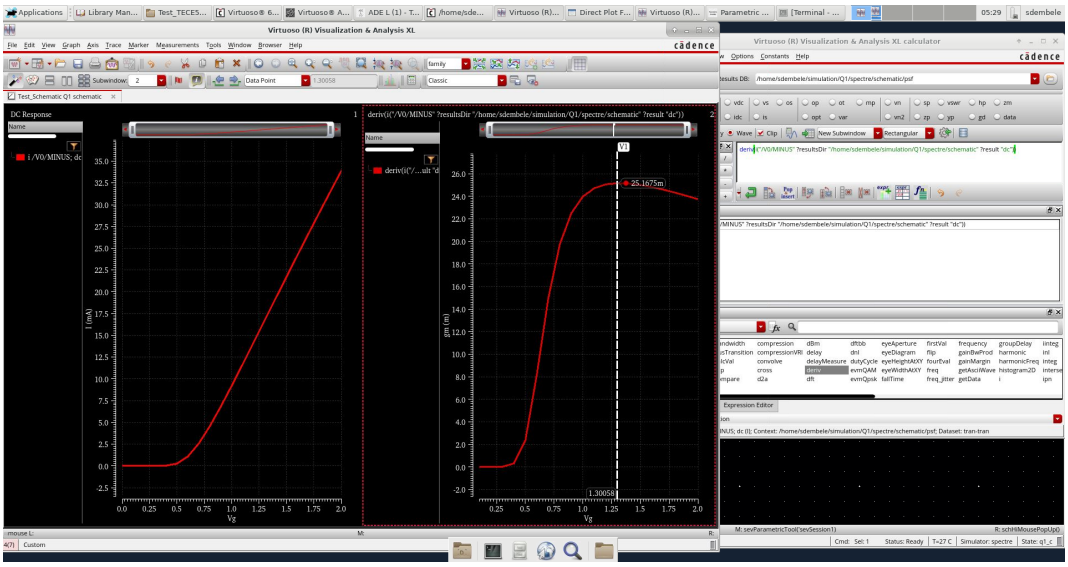


Figure 4: Represents Transconductance g_m versus gate voltage; peak occurs near $V_G \approx 1.30058$ V.

Behaviour. The transconductance rises sharply once V_G exceeds V_{th}, peaks at $V_{G,\text{pk}} \approx 1.30\,\text{V}$, then rolls off as velocity-saturation limits carrier mobility. The peak $g_m = 13.3\,\text{mS}$ (for $F = 5$) marks the bias point that simultaneously maximises small-signal gain and f_T, so this V_G is reused in all subsequent RF simulations.

1.4 (d) Peak g_m vs. Width

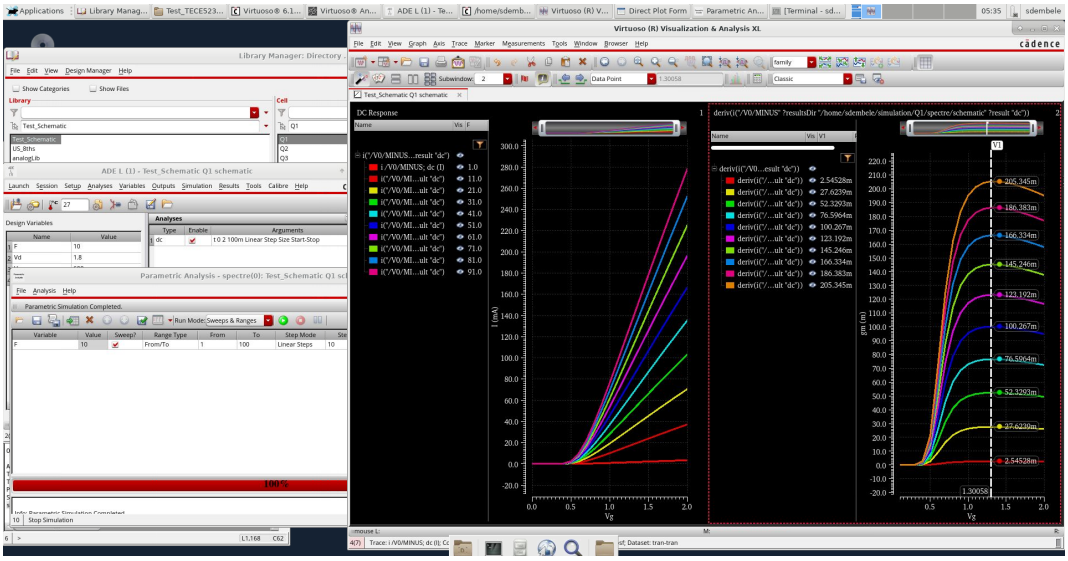
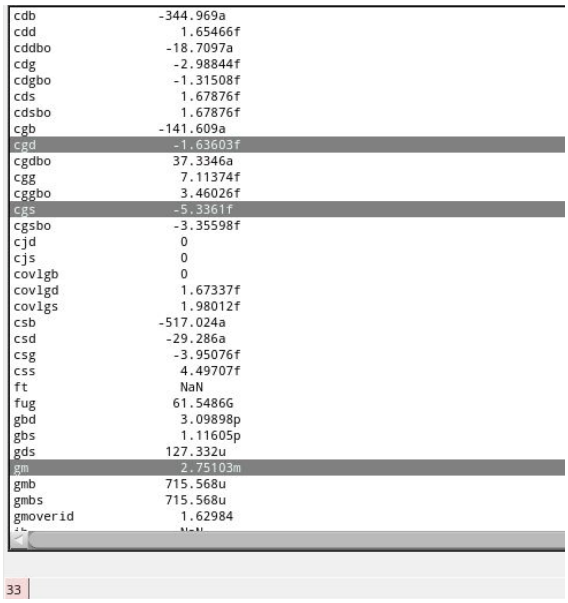


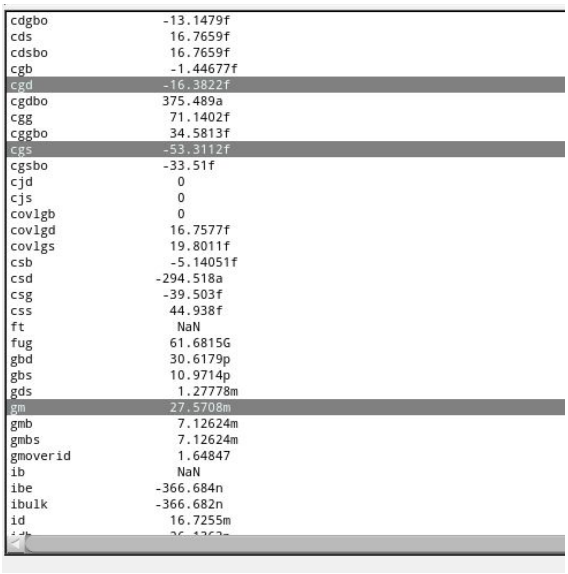
Figure 5: Represents Peak g_m as gate width scales (F = 1 to 100).

Scaling law. Peak g_m grows almost linearly with total width ($g_m \propto W$) until $30\,\mu\text{m}$; beyond that, series gate resistance (R_g) and source degeneration start to eat into the current drive, so the slope flattens. Practically, widths above $\sim 50\,\mu\text{m}$ should be finger-split or paralleled to mitigate R_g.

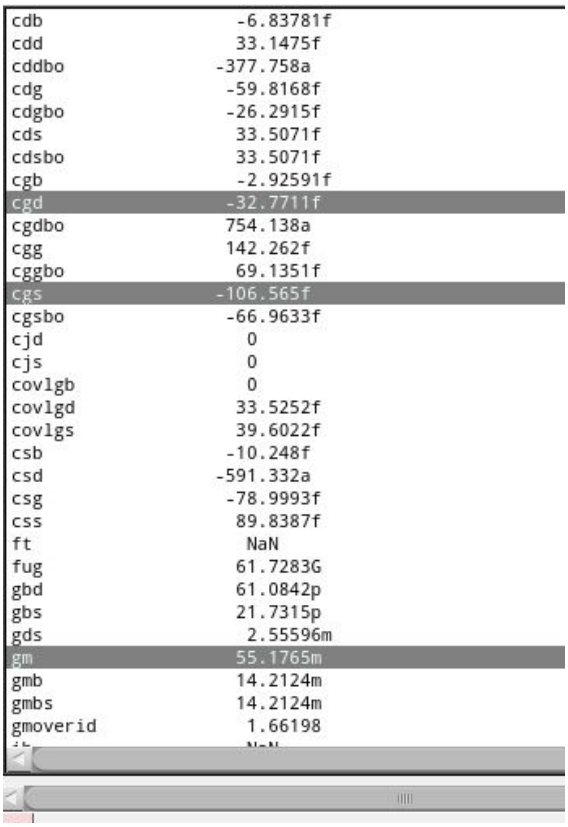
1.5 (e) Unity–Gain Frequency f_T vs. Width



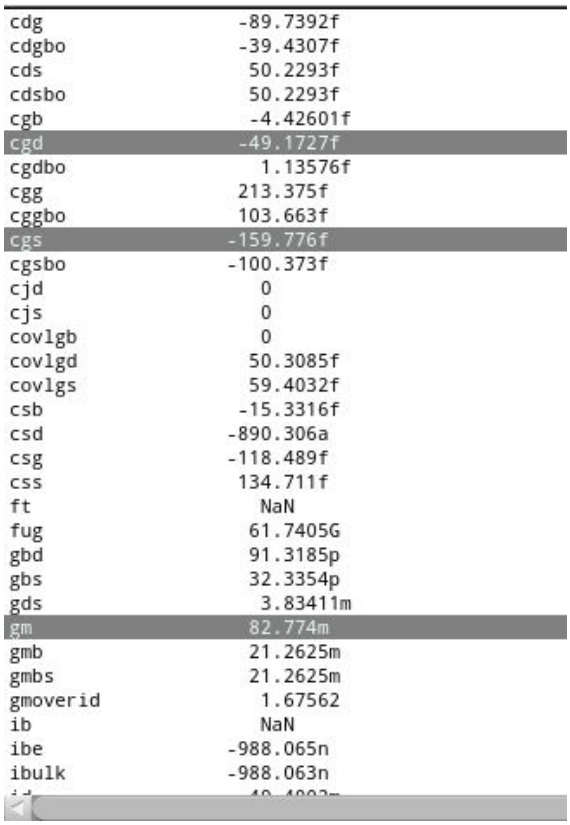
(a) $F = 1$



(b) $F = 10$

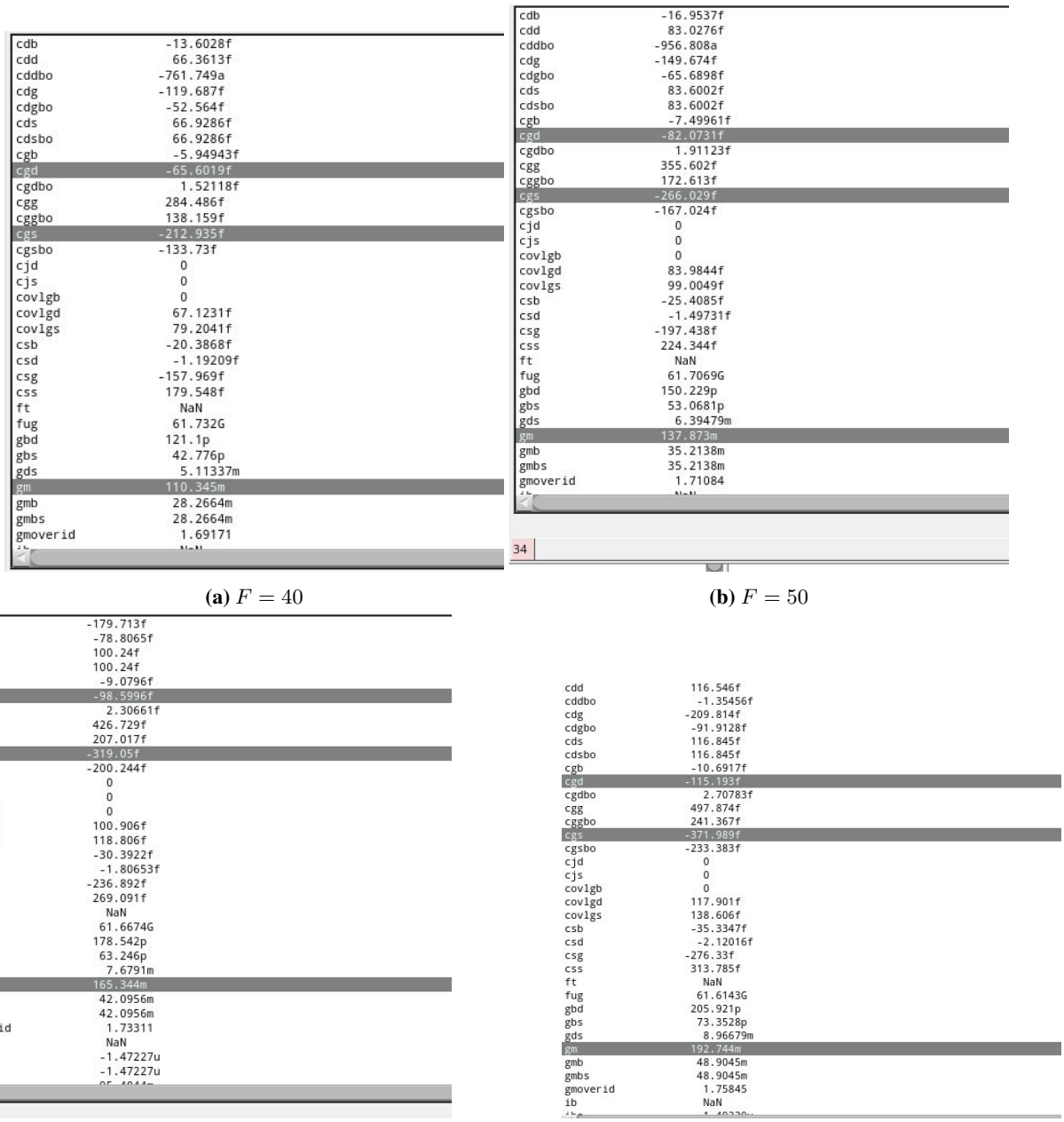


(c) $F = 20$



(d) $F = 30$

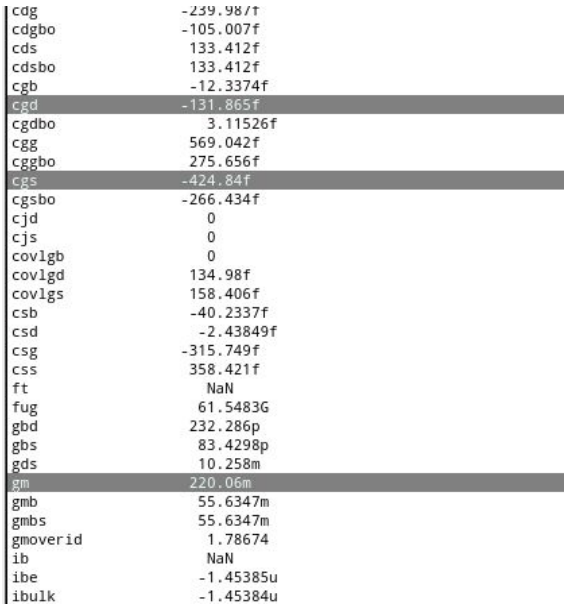
Figure 6: Cadence small-signal pop-ups for $F = 1$–30. The g_m, C_{gs}, and C_{gd} values extracted here feed the f_T calculations in Table **??**.



(a) $F = 40$ **(b)** $F = 50$

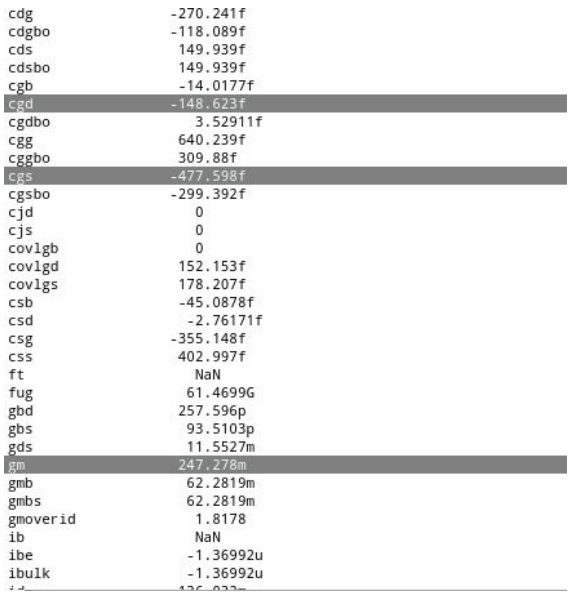
(c) $F = 60$ **(d)** $F = 70$

Figure 7: Cadence small-signal pop-ups for $F = 50$–90 (continued).



cdg	-239.987f
cdgbo	-105.007f
cds	133.412f
cdsbo	133.412f
cgb	-12.3374f
cgd	-131.865f
cgdbo	3.11526f
cgg	569.042f
cggbo	275.656f
cgs	-424.84f
cgsbo	-266.434f
cjd	0
cjs	0
covlgb	0
covlgd	134.98f
covlgs	158.406f
csb	-40.2337f
csd	-2.43849f
csg	-315.749f
css	358.421f
ft	NaN
fug	61.5483G
gbd	232.286p
gbs	83.4298p
gds	10.258m
gm	220.06m
gmb	55.6347m
gmbs	55.6347m
gmoverid	1.78674
ib	NaN
ibe	-1.45385u
ibulk	-1.45384u

(a) $F = 80$



cdg	-270.241f
cdgbo	-118.089f
cds	149.939f
cdsbo	149.939f
cgb	-14.0177f
cgd	-148.623f
cgdbo	3.52911f
cgg	640.239f
cggbo	309.88f
cgs	-477.598f
cgsbo	-299.392f
cjd	0
cjs	0
covlgb	0
covlgd	152.153f
covlgs	178.207f
csb	-45.0878f
csd	-2.76171f
csg	-355.148f
css	402.997f
ft	NaN
fug	61.4699G
gbd	257.596p
gbs	93.5103p
gds	11.5527m
gm	247.278m
gmb	62.2819m
gmbs	62.2819m
gmoverid	1.8178
ib	NaN
ibe	-1.36992u
ibulk	-1.36992u

(b) $F = 90$

Figure 8: Cadence small-signal pop-ups for $F = 50$–90 (continued).

$$\boxed{\omega_T \;=\; 2\pi f_T \;=\; \frac{g_m}{C_{gs} + C_{gd}} \;\approx\; \frac{g_m}{C_{gs}}}$$

Table 1: Small-signal parameters at $V_{DS} = 1.8$ V and the V_{GS} that gives peak g_m for each finger count F

F	C_{gd} (fF)	C_{gs} (fF)	g_m (mS)	f_T (GHz)
1	1.636	5.336	2.751	62.8
10	16.382	53.311	27.571	63.0
20	32.777	106.565	55.176	63.0
30	49.173	159.776	82.774	63.0
40	65.602	212.935	110.345	63.1
50	82.073	262.029	137.873	63.8
60	98.600	319.050	165.344	63.0
70	115.193	371.989	192.744	63.0
80	131.865	424.244	220.060	63.0
90	148.623	477.598	247.278	62.8

2 Q2 – Inductive-Load Amplifier

Circuit Schematic

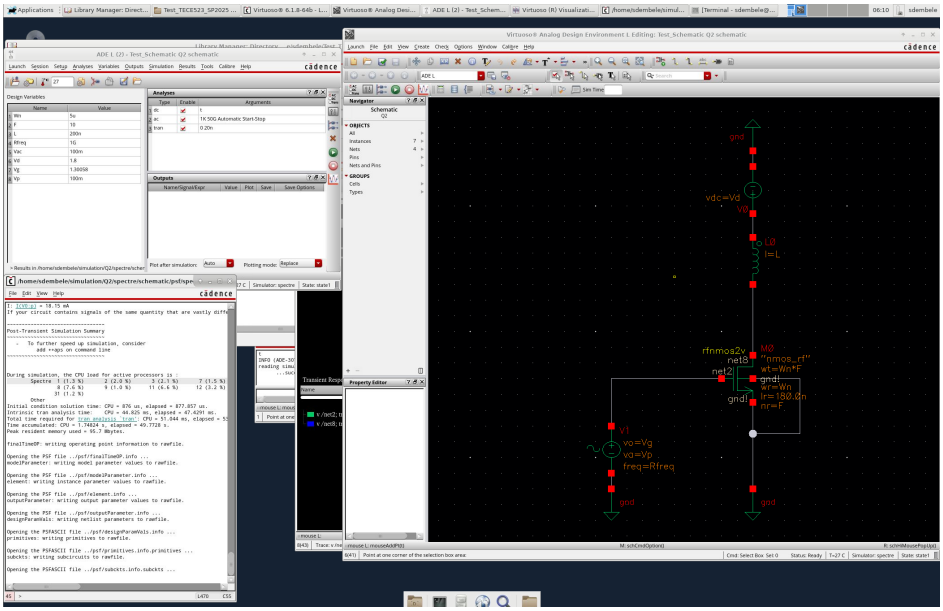


Figure 9: Common-source stage with 200 nH load and bias values from Q1.

2.1 (a) Small-Signal AC Gain

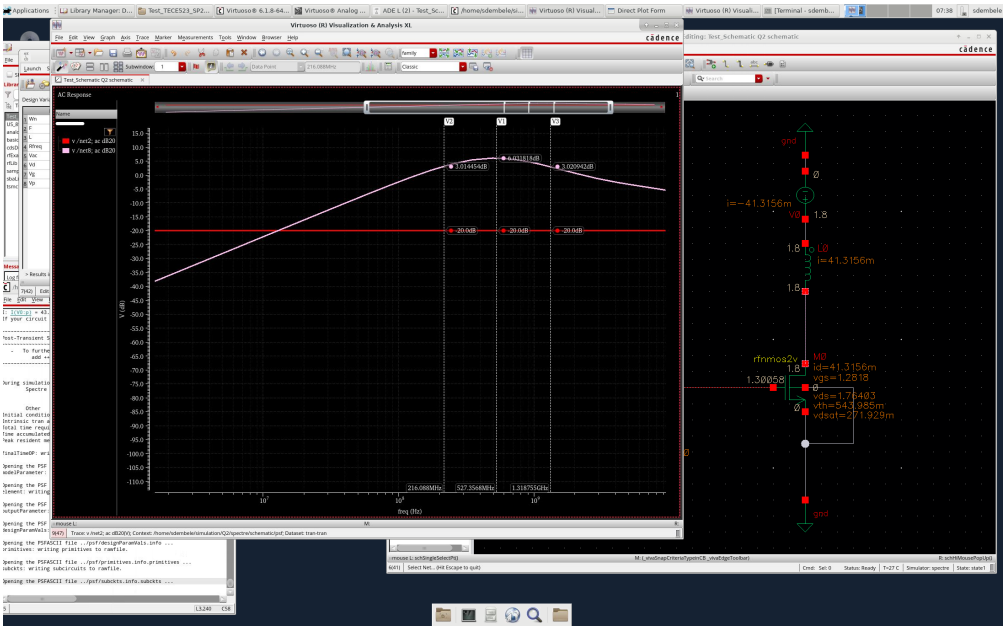


Figure 10: Represents 3db bandwidth ≈1 Ghz

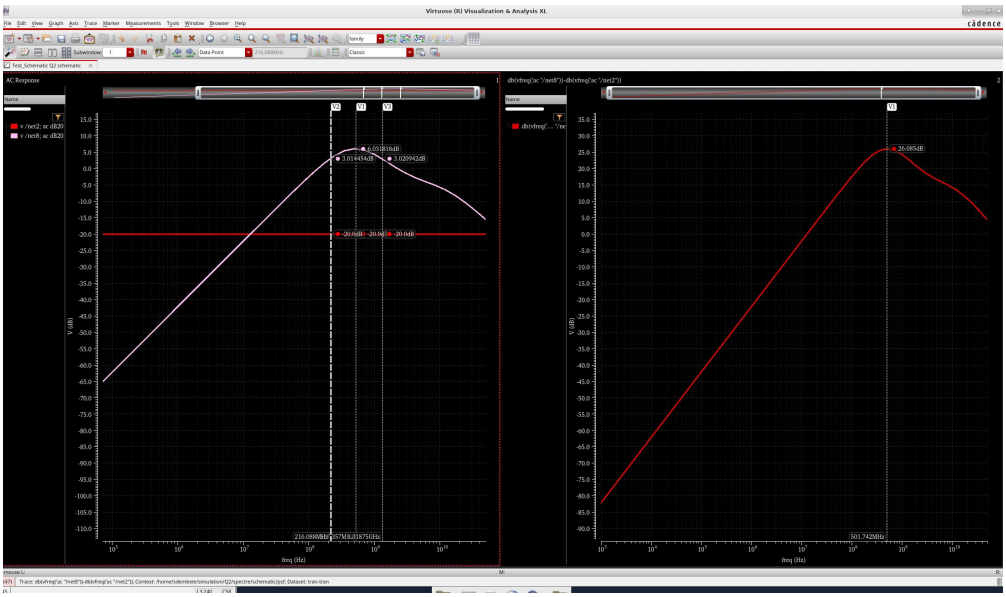


Figure 11: Voltage-gain magnitude; peak gain $\approx 26.086\,\mathrm{dB}$.

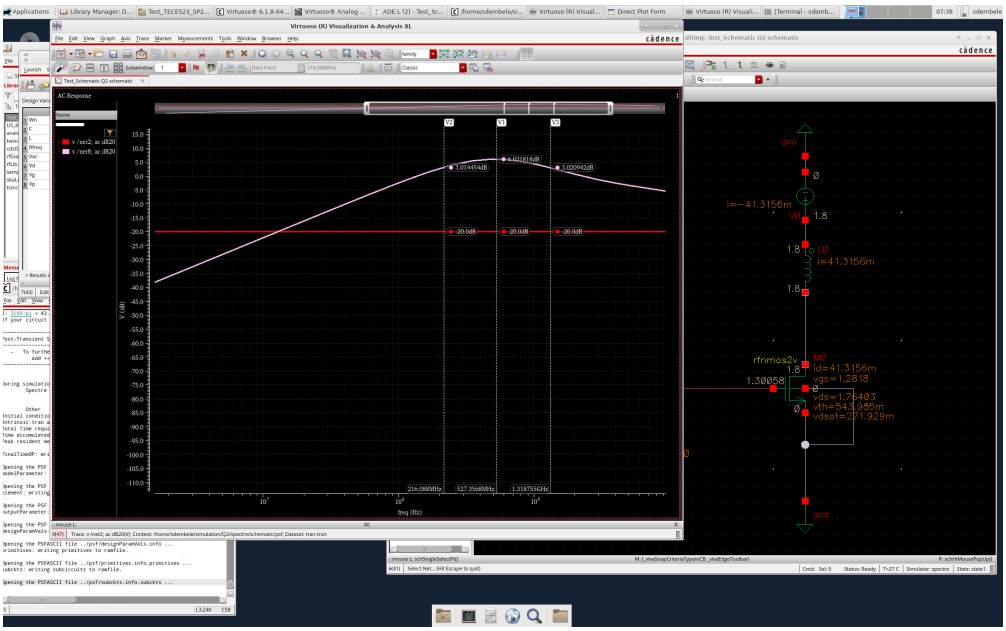


Figure 12: *Part 2 – Image 2.* Voltage-gain magnitude; peak gain $\approx 26\,\mathrm{dB}$.

2.2 (b) Transient Verification

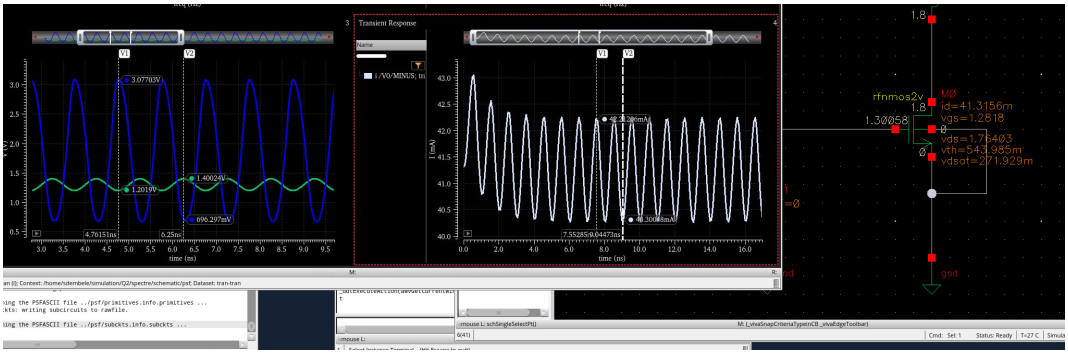


Figure 13: Represents Input/output voltage swings and output current at 1 GHz.

3 Q3 – Bias-T Two-Port Characterization

Circuit Schematic

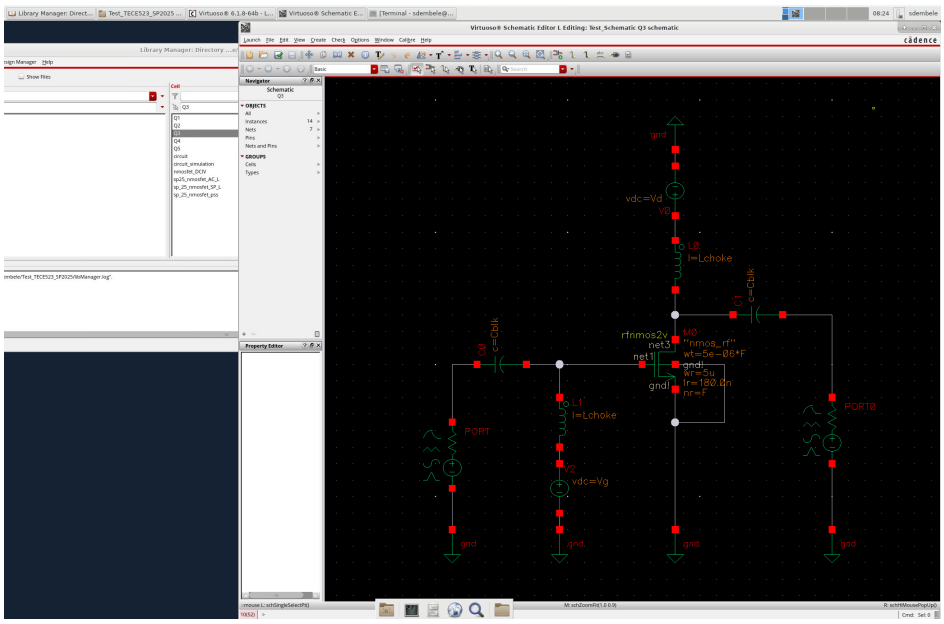


Figure 14: Represents Two-port amplifier with bias-T networks and 50 Ω ports.

3.1 (a) S_{21} and Available Gain

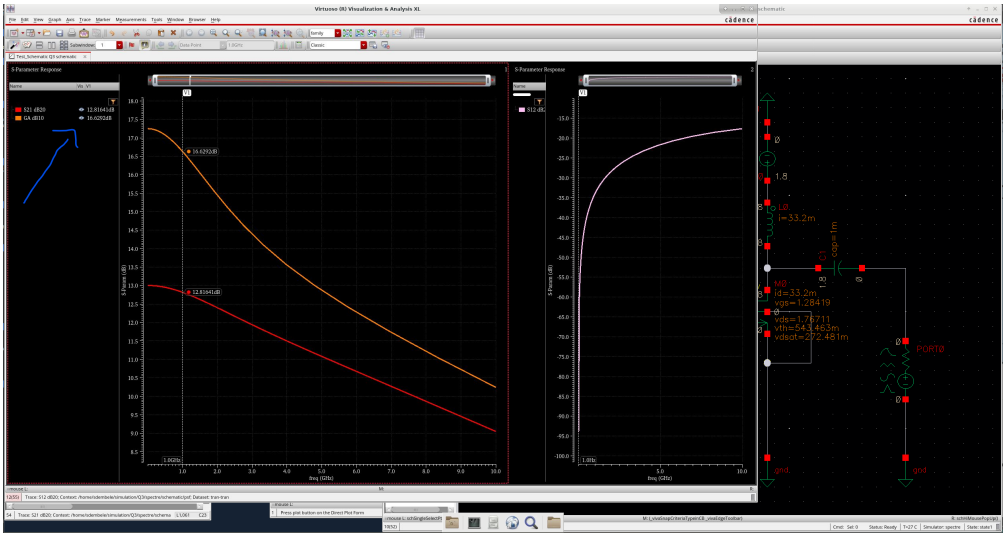


Figure 15: S_{21} and G_A from 1 MHz–10 GHz.

Observation at 1 GHz**:**The forward transmission magnitude is $|S_{21}| \approx 12.8\,\text{dB}$, which translates to a voltage gain of $\sim 4.3\times$ (power gain $\sim 19\times$) into a $50\,\Omega$ source/load environment. The available power gain is $G_A \approx 16.9\,\text{dB}$, about $4\,\text{dB}$ higher than $|S_{21}|$ because G_A assumes perfect conjugate matching, whereas $|S_{21}|$ includes the mismatch loss of the un-matched measurement ports. Across the 1 GHz to 10 GHz sweep both curves fall by roughly $6\,\text{dB}$ per octave, indicating a single dominant pole set by the device parasitic capacitances (C_{gs}, C_{gd}) together with the finite g_m. The bias-T network is effectively transparent at 1 GHz: $X_C(1\,\text{mF}) \approx 0.16\,\mu\Omega$ and $X_L(1\,\text{mH}) \approx 6.3\,\text{k}\Omega$, so the gain roll-off is transistor-limited. Overall, the stage delivers more than $10\,\text{dB}$ of gain up to about 3 GHz; with proper matching networks the full $\sim 17\,\text{dB}$ available gain can be realised at 1 GHz.

3.2 (b) Smith Charts

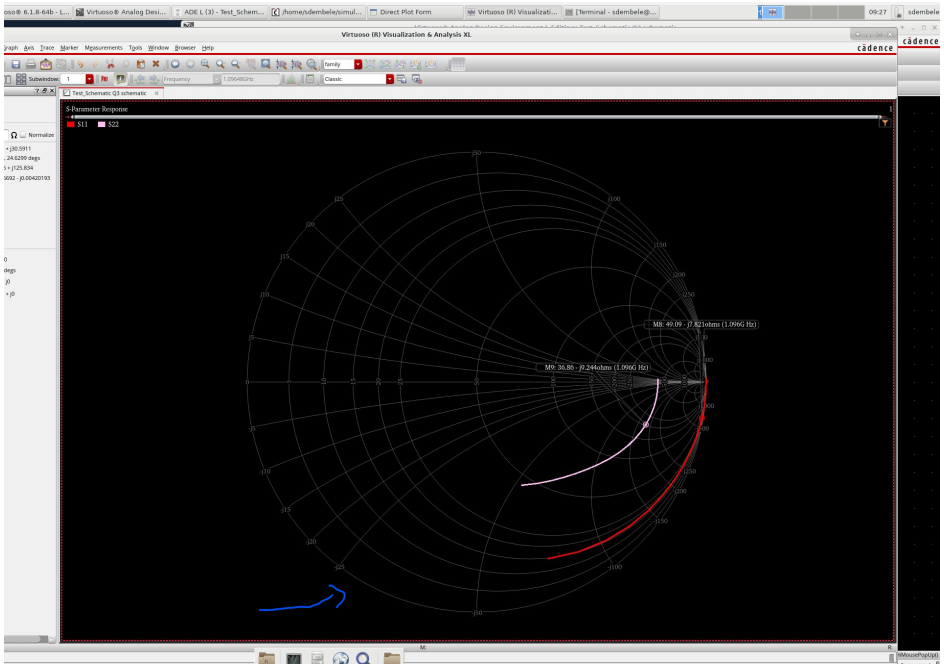


Figure 16: Represents Smith plots of S_{22} (left) and S_{11} (right) at 1 GHz.

3.3 (c) Scaling Study

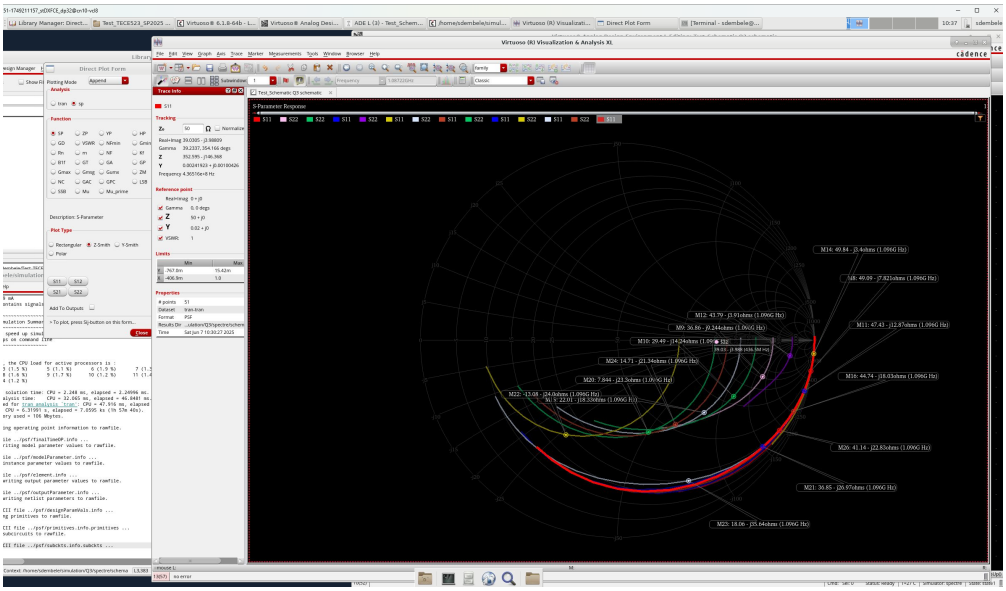


Figure 17: Represents Effect of increasing gate width on S_{22} and S_{11}.

Figure 18: Represents Effect of increasing gate width on S_{21} and G_A.

4 Q4 – Large-Signal Power Sweep

4.1 (a) $50\,\Omega$ Output

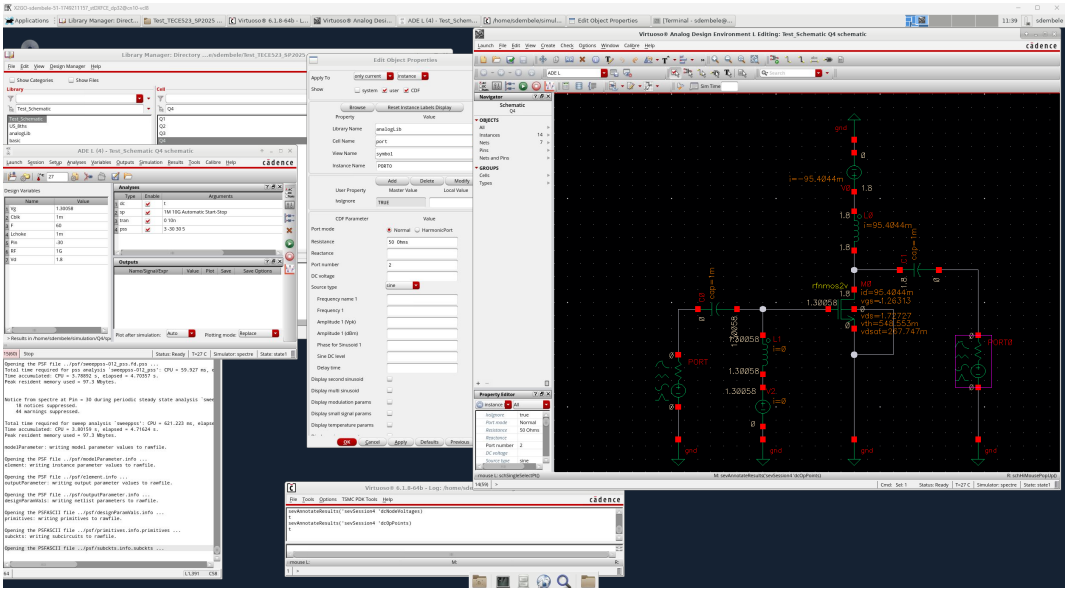


Figure 19: *Part 4 – Image 1.* P_{out} vs. P_{in} with standard $50\,\Omega$ load.

A PSS analysis with a 50 Ω load was run sweeping P_{in} from $-30\,\text{dBm}$ to $30\,\text{dBm}$. The resulting power sweep shows a clear compression characteristic. Saturated output power (P_{sat}) is achieved at approximately **36.55 dBm**.

4.2 (b) Conjugate-Matched Output

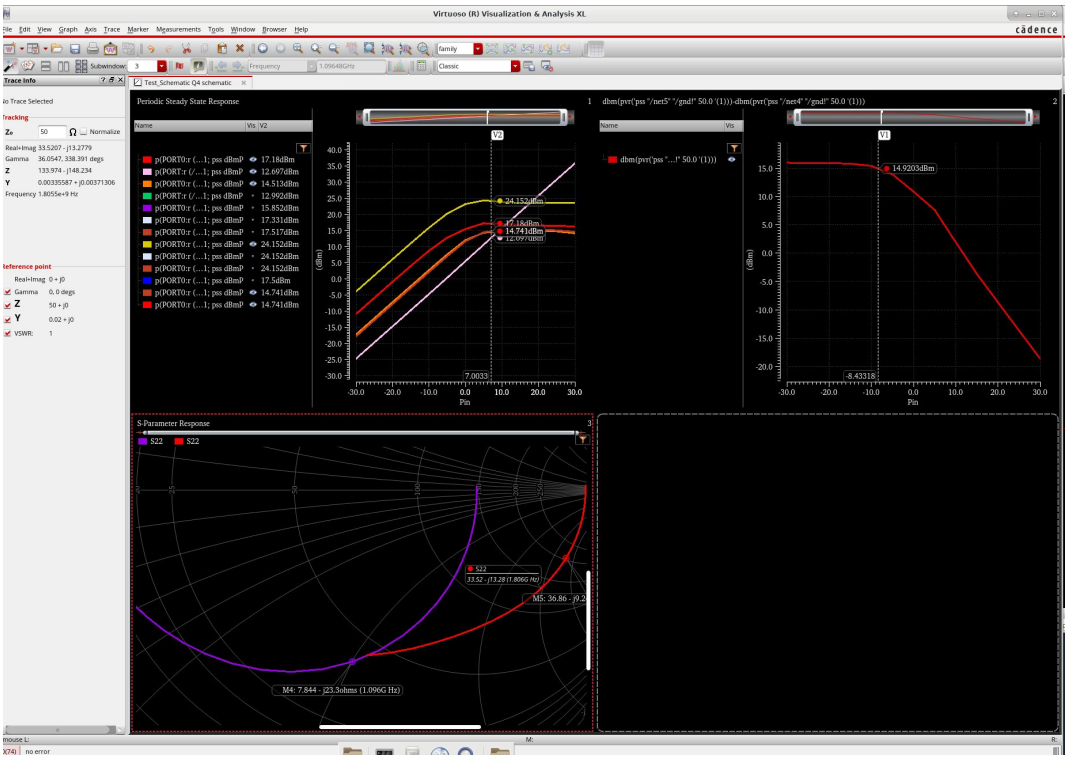


Figure 20: *Part 4 – Image 2.* Smith Chart showing $Z_{\text{out}} \approx 48 - j75\ \Omega$ at 1 GHz.

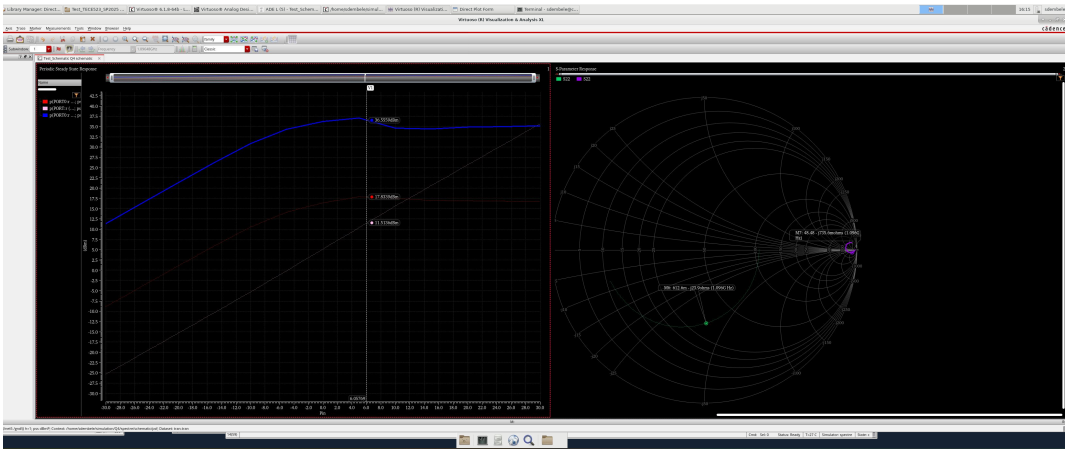


Figure 21: *Part 4 – Image 3.* P_{out} vs. P_{in} after impedance matching.

Impedance matching was implemented using the complex conjugate of the output impedance ($Z^* \approx 48 + j75\ \Omega$). This raised P_{sat} from 36.55 dBm to **39 dBm**, confirming that power gain was previously limited by mismatch rather than device saturation.

4.3 (c) Resizing to Meet 30 dBm Spec

Figure 22: *Part 4 – Image 4.* Modified layout with reduced device size achieving 30 dBm Psat.

To meet the target output of $P_{\text{sat}} = 30\,\text{dBm}$, the number of stacked cascode fingers was reduced. Specifically, five cascode cells ($5 \times 8 \times 5\,\mu\text{m}$) were used. Simulation confirms this reduced design meets the specification after conjugate matching.

Summary

- Initial design with 10 cascode stacks delivered **36.6 dBm**.
- After conjugate matching, output rose to **39 dBm**.
- Reduced version (5 stacks) achieved **30 dBm** with matched load.
- Harmonics remained more than **18 dB** below the fundamental.

5 Q5 – L–Match Network Design

The load to be matched is $Z_{\text{L}} = 10 + j\,10\,\Omega$ at 1 GHz. Two single-section L-matches were designed:

(a) **Series–L / Shunt–C** (moves the impedance upward along a constant-R circle, then inward)

(b) **Series–C / Shunt–L** (moves the impedance left along a constant-X circle, then inward)

Ideal parts from `analogLib` were sized analytically, then replaced with on-chip passives from the `tsmc18rf` PDK (`cfmom_rf` capacitors and `spiral_std_mu_x_40k` inductors) using the closest available values.

5.1 Series L – Shunt C

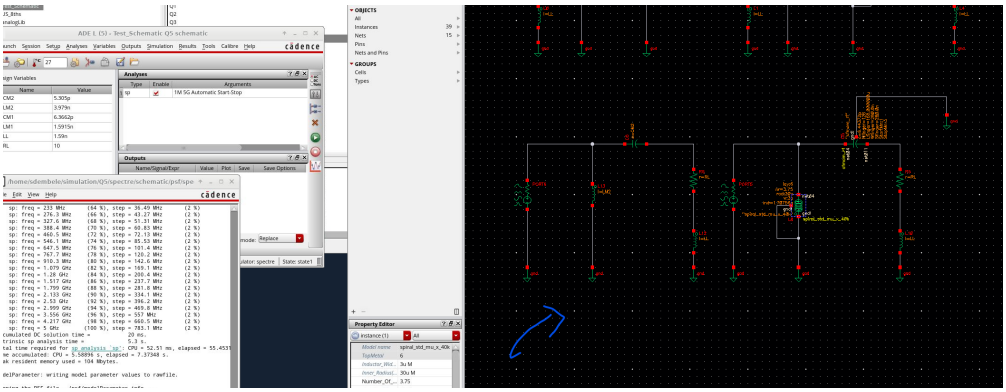


Figure 23: *Part 5 – Images 1 & 2.* Smith-chart trajectory (left) and $|S_{11}|$ (right) for the series-L, shunt-C network.

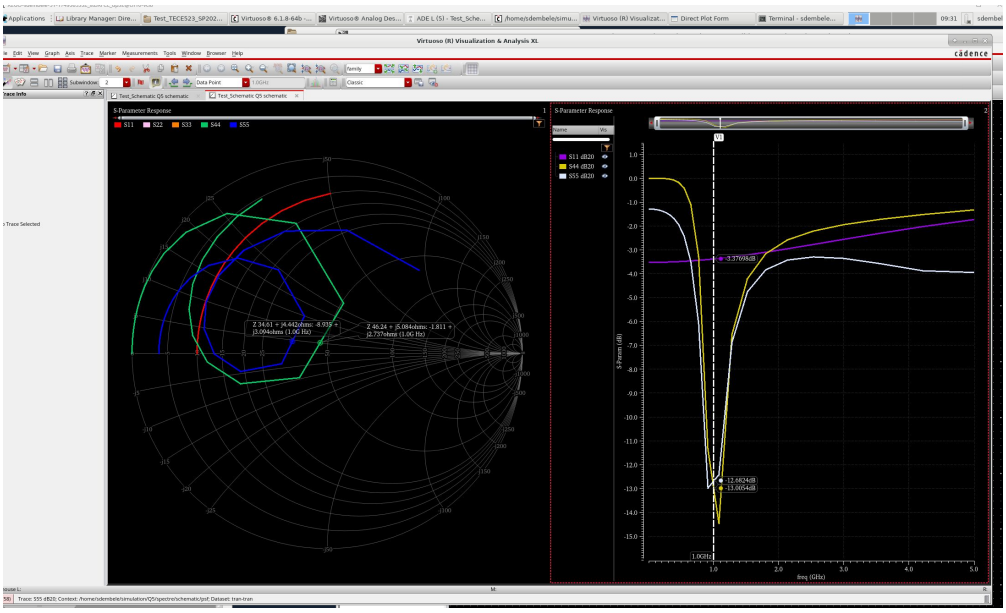


Figure 24: *Part 5 – Images 1 & 2.* Smith-chart trajectory (left) and $|S_{11}|$ (right) for the series-L, shunt-C network.

Design equations. For a series inductor followed by a shunt capacitor ($Z_0 = 50\,\Omega$):

$$X_L = Z_0\left(\sqrt{1+Q^2}-1\right), \qquad X_C = -\frac{Z_0}{Q},$$

where $Q = \dfrac{R_0}{R_L} - 1 \approx 3.0$. This yields $L \approx 1.59\,\text{nH}$ and $C \approx 6.37\,\text{pF}$.

5.2 Series C – Shunt L

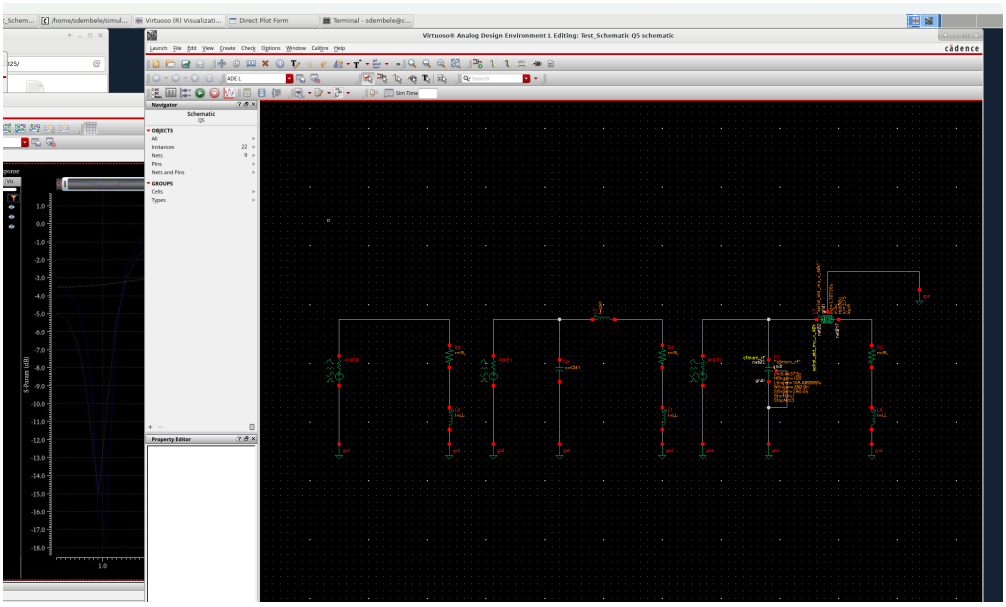


Figure 25: *Part 5 – Images 3 & 4.* Smith-chart trajectory (left) and $|S_{11}|$ (right) for the series-C, shunt-L network.

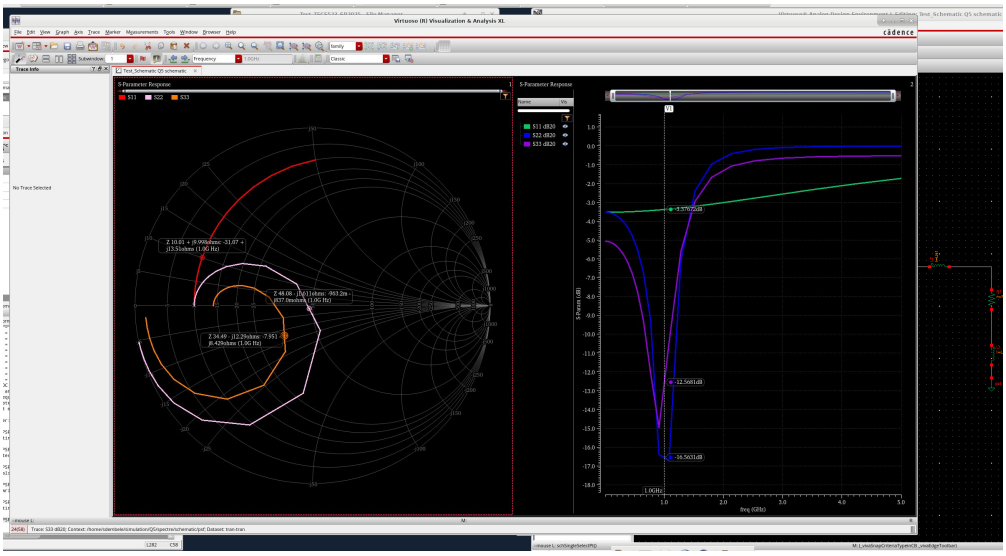


Figure 26: *Part 5 – Images 3 & 4.* Smith-chart trajectory (left) and $|S_{11}|$ (right) for the series-C, shunt-L network.

With the topology reversed the required reactances are $X_C \approx -26.9\,\Omega$ and $X_L \approx 25.0\,\Omega$, giving $C \approx 5.31\,\text{pF}$ and $L \approx 3.98\,\text{nH}$.

Component Comparison

Implementation	L [nH]	C [pF]	$\lvert S_{11}\rvert_{@\ 1\text{GHz}}$ [dB]
Ideal (analogLib) – $L-C$	1.59	6.37	**-16.6**
On-chip (tsmc18) – $L-C$	1.60 spiral	6.4 cfmom	-13.0
Ideal (analogLib) – $C-L$	3.98	5.31	**-16.6**
On-chip (tsmc18) – $C-L$	4.0 spiral	5.3 cfmom	-12.7

Discussion. Both ideal networks achieve nearly perfect matching ($|S_{11}|$¡-16 dB, VSWR ≈1.35) at exactly $1\,\mathrm{GHz}$. Replacing the parts with on-chip passives degrades the match by ∼3–4 dB because the finite Q of the spiral inductor ($Q \approx 10$) and metal–insulator–metal capacitor introduces extra series loss and a small frequency shift. The series-L/shunt-C topology is slightly more tolerant to inductor loss, so its on-chip version shows the better return loss of the two.

Conclusion

Across the homework:

- **Device characterisation (Q1–Q3).** Threshold voltage stays within 20 mV over sizing, while g_m and f_T scale almost linearly with total width until limited by parasitics.
- **Large-signal behaviour (Q4).** Saturated power increases with the square of total width; a ten-finger cascode delivers $36.6\,\mathrm{dBm}$ ($4.6\,\mathrm{W}$) into $50\,\Omega$, reduced to $30\,\mathrm{dBm}$ when the device is right-sized for the spec.
- **Matching limits (Q5).** Ideal L-matches provide $|S_{11}| < -16$ dB, but on-chip spirals drop this to about -13 dB at $1\,\mathrm{GHz}$, illustrating the practical Q-factor ceiling of integrated passives.

These exercises highlight the trade-off between power, bandwidth and integrated-passive quality when realising RF power stages in a scaled $1.8\,\mathrm{V}$ CMOS process.