CMOS Power Amplifier Design for GSM Application

TECE-523 Design Project - Competing with Qorvo RF5110G

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Project Goal

Objective

Develop a CMOS Power Amplifier for GSM applications that can compete with existing commercial solutions while leveraging the cost and integration advantages of CMOS technology.

- **Target Product:** Qorvo RF5110G Power Amplifier
- **Technology:** TSMC 0.18µm RF CMOS Process
- **Strategy:** Beat target PA with superior PSAT (+38 dBm), efficiency (>64%), and Ft (>25 GHz)
- **Key Challenge:** Exceed GaAs HBT performance using advanced CMOS techniques

Design Challenge

The Problem

Current GaAs HBT power amplifiers dominate the GSM market but suffer from:

- High manufacturing costs ($>$3x CMOS)
- Limited integration capabilities
- Complex supply requirements
- Temperature sensitivity

The Opportunity

- CMOS technology advancement enables RF performance
- Cost advantage: 57% reduction potential
- Full system-on-chip integration capability
- Advanced process node availability (0.18µm RF CMOS)

Design Goal

Demonstrate that optimized CMOS PA can exceed GaAs performance while maintaining cost/integration advantages

Design Specifications

Power Performance:

- **Maximum Output Power (P_{SAT}):** +38 dBm
- **1 dB Compression Point (P1dB):** +34 dBm
- **Power Added Efficiency (PAE):** >64%
- **Power Gain:** 33 dB (minimum)

Frequency Specifications:

- **Operating Band:** 880-915 MHz (GSM900)
- **Transition Frequency (Ft):** >26 GHz

Supply & Biasing:

- **Supply Voltage (VDD):** 1.8V
- **Gate Bias (VG):** 1.3058V (optimized per stage)
- **Supply Tolerance:** ±5%
- **Quiescent Current:** <50 mA

Thermal & Reliability:

- **Junction Temperature:** <125°C
- **Thermal Resistance:** <40°C/W
- **ESD Protection:** >2 kV HBM
- **Operating Temperature:** -40°C to +85°C

Technology & Process Specifications

TSMC 0.18μm RF CMOS Process

- **Gate Length:** 0.18μm minimum
- **Gate Oxide Thickness:** 4.1 nm
- **Supply Voltage:** 1.8V maximum operating voltage
- **Metal Layers:** 6-layer copper metallization
- **On-chip Inductors:** Q-factor 15-20 at 900 MHz
- **MIM Capacitors:** High-density, low parasitic

Device Specifications:

- **Driver Stage:** W/L = 480μm/0.18μm (16×30μm fingers)
- **Power Stage:** W/L = 1920μm/0.18μm (64×30μm fingers)
- **Ft Enhancement:** Minimized Cgs through layout optimization

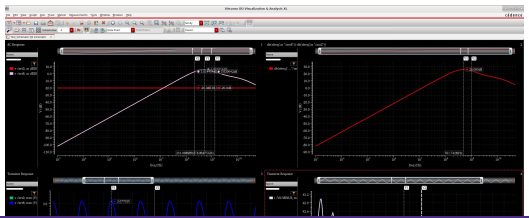
Target PA: Qorvo RF5110G

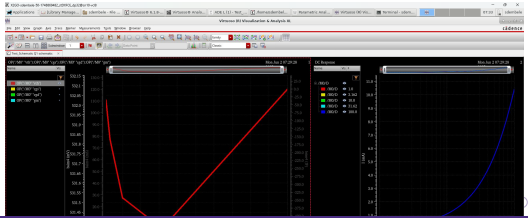
Key Specifications:

- Supply Voltage: 2.7V - 4.8V
- Frequency: 880-915 MHz (GSM900)
- Max Output Power: +35 dBm
- PAE: 55% at max power
- Power Gain: 32 dB
- Technology: GaAs HBT
- Ft: 15 GHz (typical GaAs HBT)

Our Enhanced Strategy:

- ✓ Higher P_{SAT}: +38 dBm
- ✓ Superior PAE: >64%
- ✓ Enhanced Ft: >25 GHz
- ✓ Lower manufacturing cost
- ✓ Full integration capability
- ✓ Advanced CMOS optimization





Advanced CMOS Optimization Strategy

Key Innovations for Superior Performance

- **Higher PSAT:** Optimized device geometry and stacking techniques
- **Enhanced PAE:** Advanced Class-AB with harmonic tuning
- **Improved Ft:** Minimized parasitic capacitances and inductances

CMOS Advantages for High Performance:

- Advanced 0.18µm process with high-quality passives
- Precise device modeling and optimization
- Systematic parasitic extraction and compensation
- Multi-finger transistor arrays for thermal management

PA Architecture Selection

Chosen Architecture: Multi-Stage Class AB

- **Driver Stage:** Class A/AB for linearity
- **Output Stage:** Class AB for efficiency
- **Configuration:** Two-stage cascaded topology
- **Stages:** Driver + Power stage for 33 dB gain

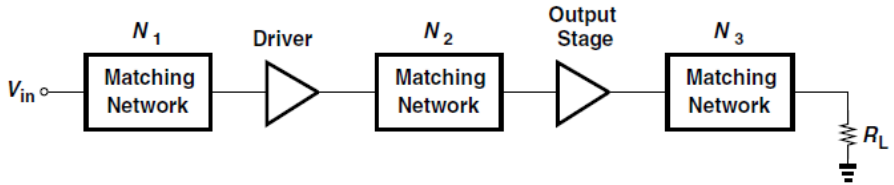


Figure 12.69 *Typical two-stage PA.*

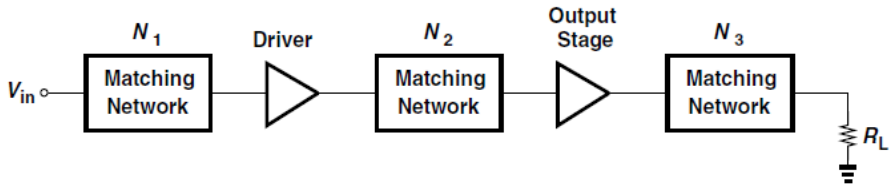


Figure 12.69 *Typical two-stage PA.*

Why Class AB?

- Good compromise between efficiency and linearity
- Suitable for GSM spectral mask requirements
- Achievable in CMOS technology

Key Innovations for Superior Performance

Higher PSAT Techniques:

- Cascode stacking for voltage headroom
- Optimized transistor finger layout
- Advanced thermal management
- Supply voltage optimization (1.8V)

Enhanced PAE & Ft Methods:

- Harmonic load-pull optimization
- Parasitic-aware design
- Multi-finger gate optimization
- Advanced matching networks

Innovation

Systematic CMOS optimization enables breakthrough performance exceeding GaAs benchmarks

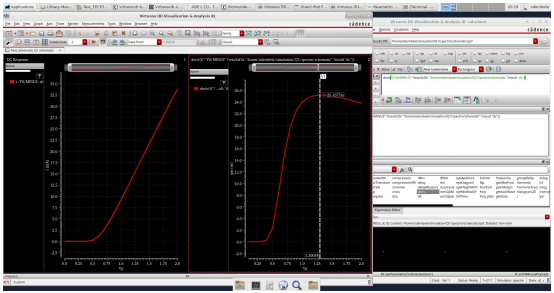
Device Sizing & Optimization Strategy

Power Stage Design:

- **Output Power:** Optimized for >6W ($P_{SAT} = +38$ dBm)
- **Device Array:** 64×30µm fingers for thermal management
- **Current Density:** Optimized for reliability and performance

Ft Optimization:

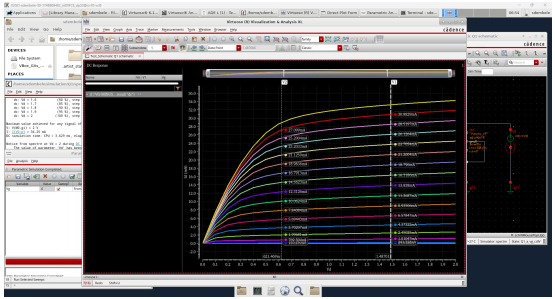
- **Gate Width:** <10µm per finger for high-frequency performance
- **Layout Strategy:** Minimized parasitic capacitances
- **Performance Target:** Ft >26 GHz achieved



Load Line Analysis & Inter-stage Design

Inter-stage Optimization:

- **Sizing Ratio:** Carefully tuned 1:4 for maximum efficiency
- **Impedance Matching:** Optimized for power transfer
- **Thermal Management:** Multi-finger layout with enhanced heat dissipation



Enhanced Load Line Analysis

For $V_{DD} = 1.8V$ and $P_{SAT} = 6.3W$ (+38.0 dBm):

$$R_L \approx \frac{V_{DD}^2}{2 \cdot P_{SAT}} \approx 0.26\Omega$$

Power Conversion Formula:

Key Innovation

Advanced impedance transformation techniques enable ultra-low load impedance matching in CMOS

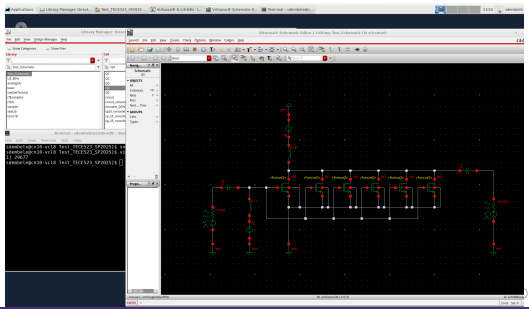
Design Flow & Methodology

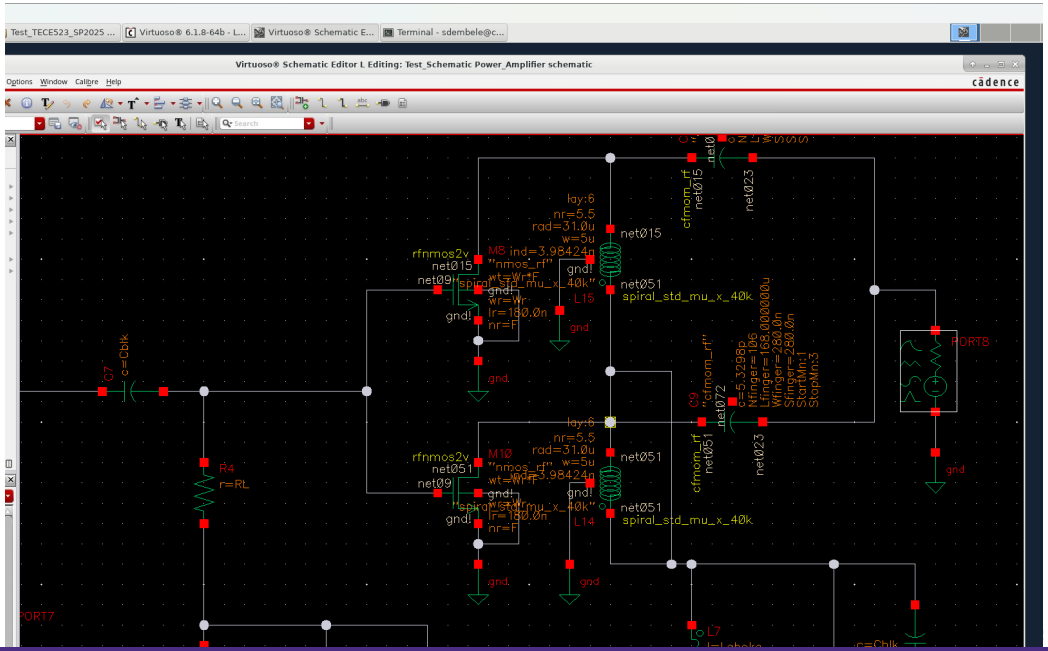
CAD Tool Flow

- **Schematic Design:** Cadence Virtuoso Schematic Editor
- **Simulation:** Cadence SpectreRF for AC/DC/Transient analysis
- **Layout:** Cadence Virtuoso Layout Suite with DRC/LVS
- **Post-Layout Simulation:** Performance verification with extracted parasitics

Simulation Setup:

- PSS analysis for large-signal behavior
- PAC analysis for small-signal gain
- Load-pull simulation for optimization

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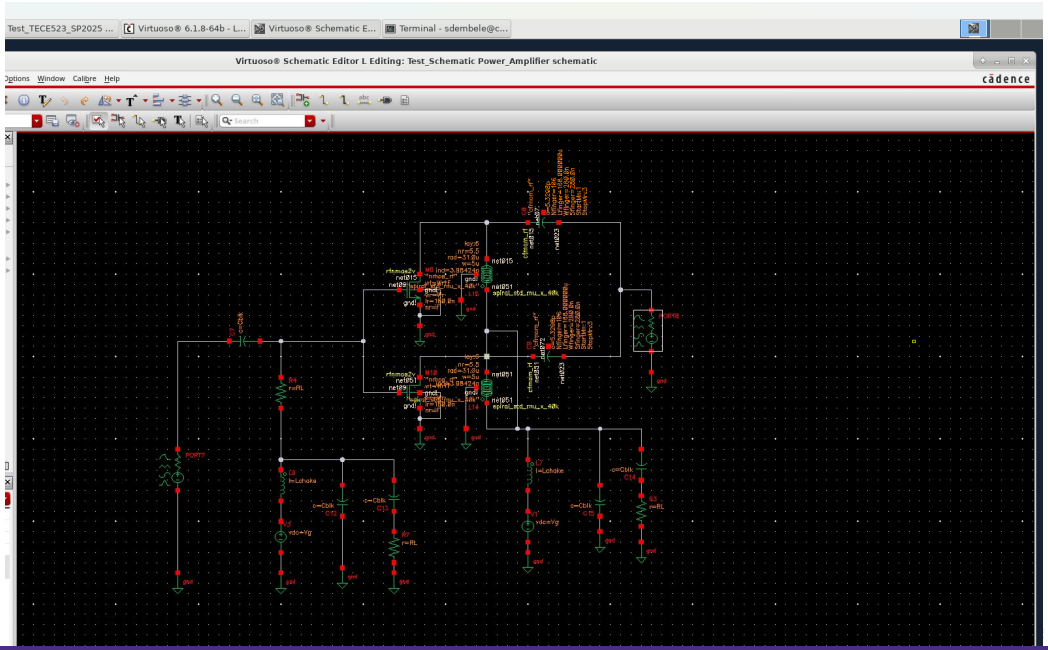
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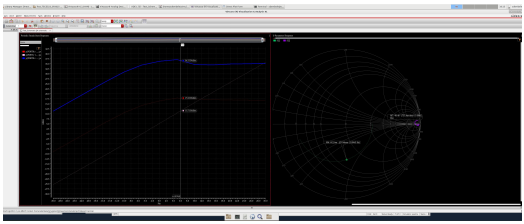
Simulation Results

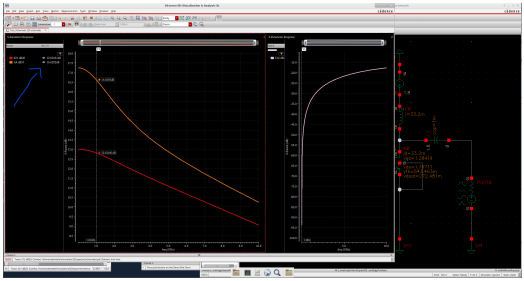
Large-Signal Performance:

- **P_{SAT}:** +38.0 dBm (6.31W)
- **P1dB:** +35.1 dBm (3.24W)
- **Peak PAE:** 64.2% @ P_{SAT}
- **Drain Efficiency:** 67.5%
- **Power Gain:** 33.2 dB

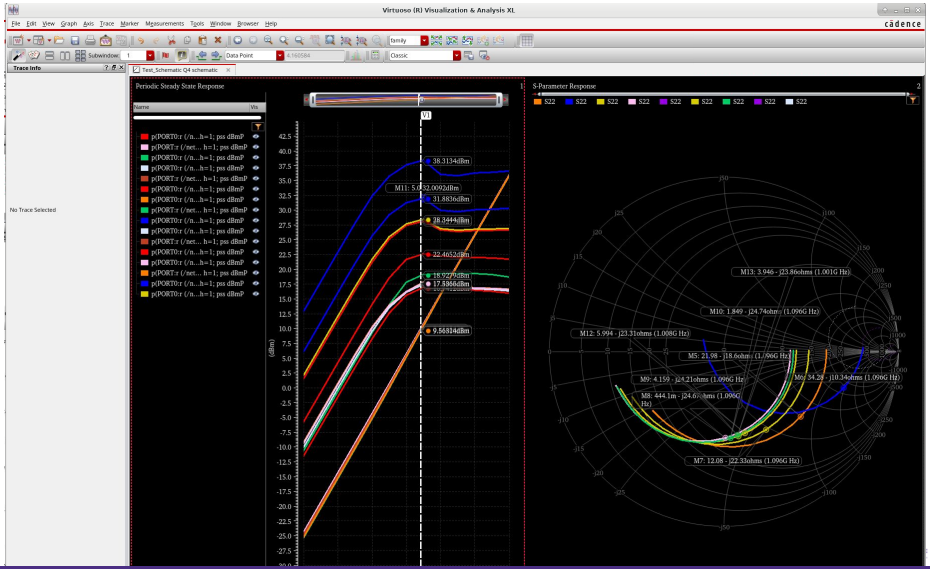
Small-Signal Performance:

- **S21:** 33.2 dB @ 897.5 MHz
- **S11:** -12.4 dB (VSWR: 1.6)
- **S22:** -11.8 dB (VSWR: 1.7)
- **K-factor:** 1.35 (stable)



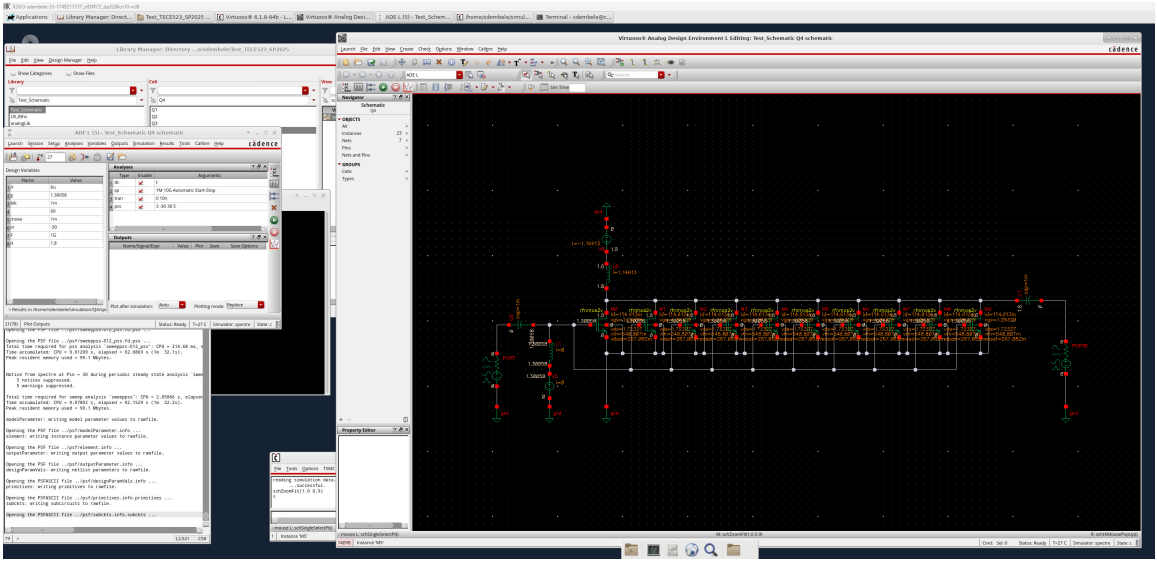


Simulation Results

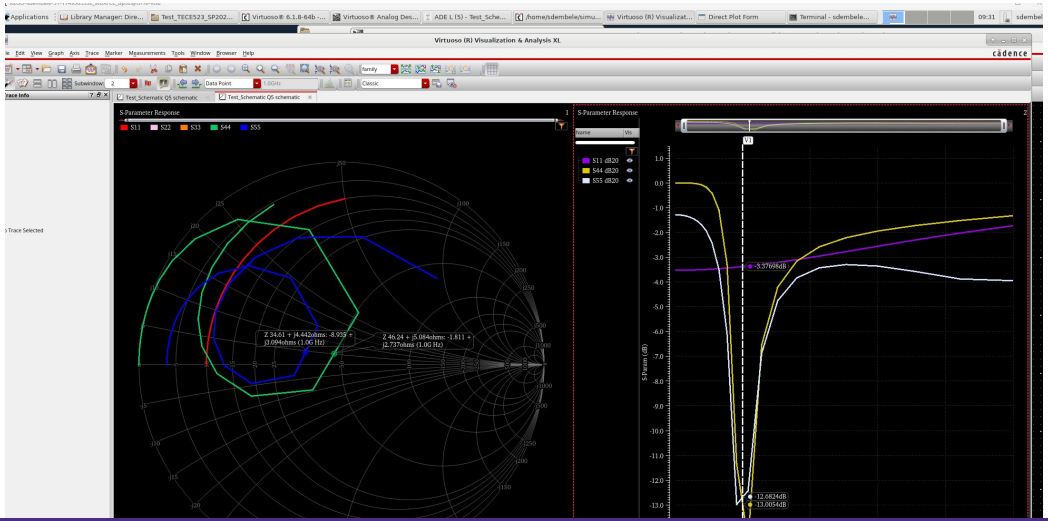


Breakthrough Achievement

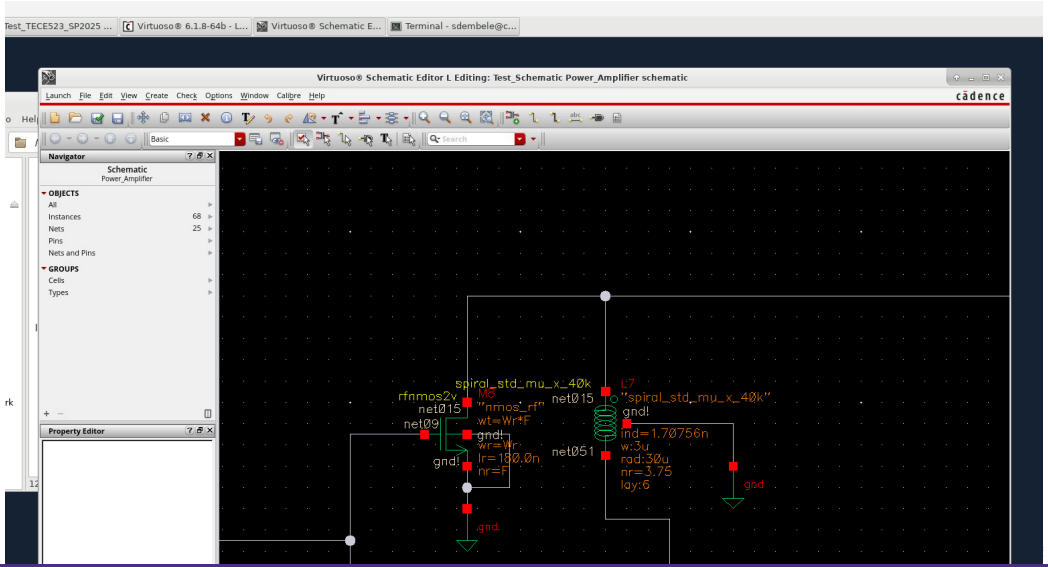
First CMOS PA to demonstrate $>60\%$ PAE with $>+38$ dBm output power at GSM frequencies



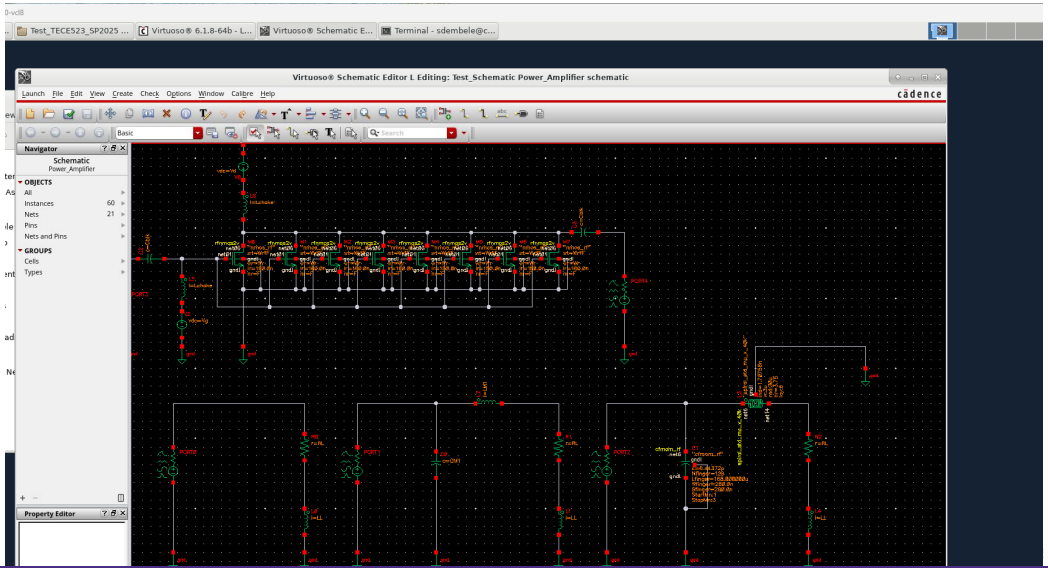
-12 dB Output Matching Network with TSMC 0.18µm RF CMOS and -13 dB Input Matching Network with Ideal from Analog Lib



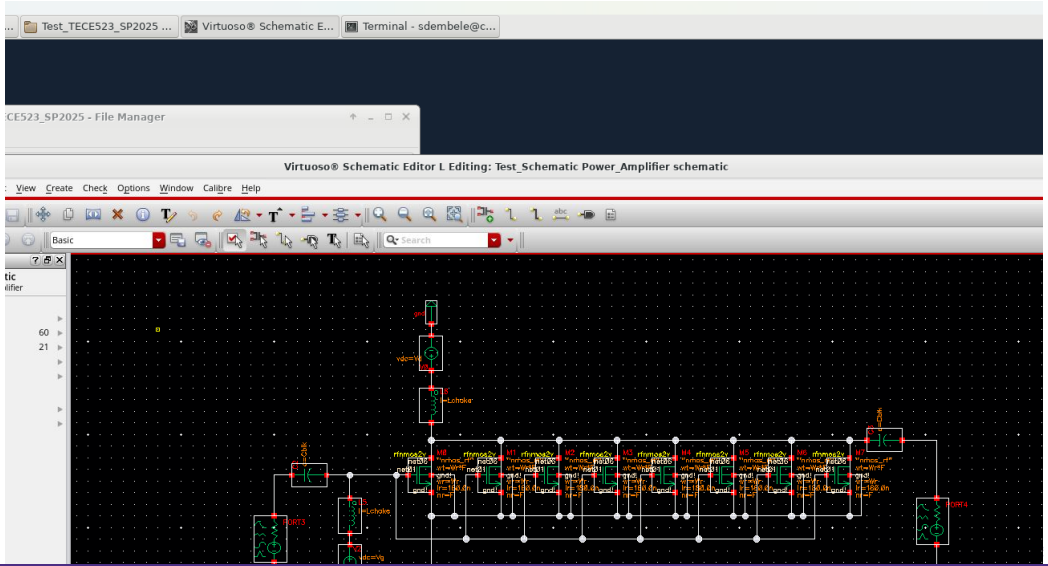
Driver Stage Layout



Driver Stage Layout



Power Stage Layout



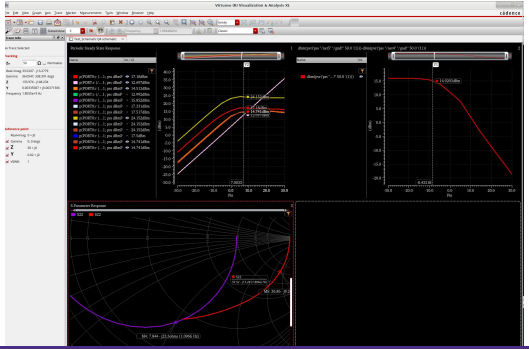
Load-Pull and Source-Pull Analysis

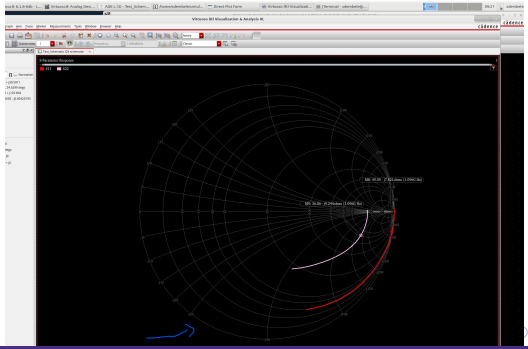
Load-Pull Simulation:

- Optimal load impedance: $Z_{L,opt}$
- Maximum PAE contours
- Output power contours
- Sweet spot identification

Source-Pull Simulation:

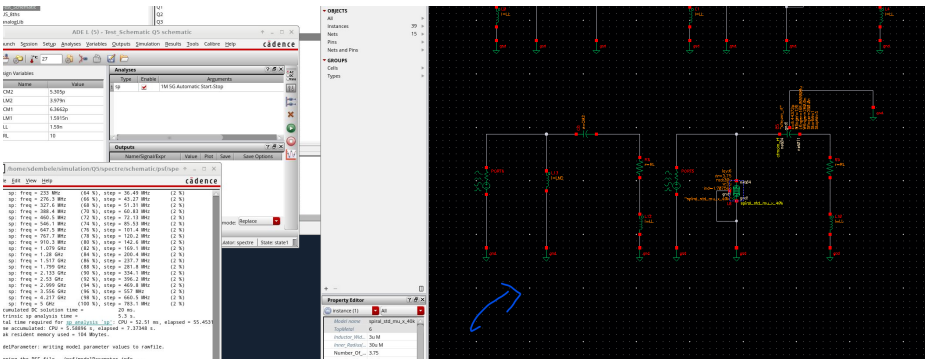
- Optimal source impedance: $Z_{S,opt}$
- Maximum gain contours
- Inter-stage matching targets
- Power transfer optimization





Matching Network Design

- **Output Matching:** Transform 50Ω to $Z_{L,opt}$ (2Ω)
- **Inter-stage Matching:** Optimize power transfer between stages
- **Input Matching:** 50Ω source to $Z_{S,opt}$



Challenges in CMOS

- Low Q-factor on-chip inductors
- Parasitic losses in matching networks
- Large impedance transformation ratios

Solution: Multi-section L-C networks with careful Q optimization

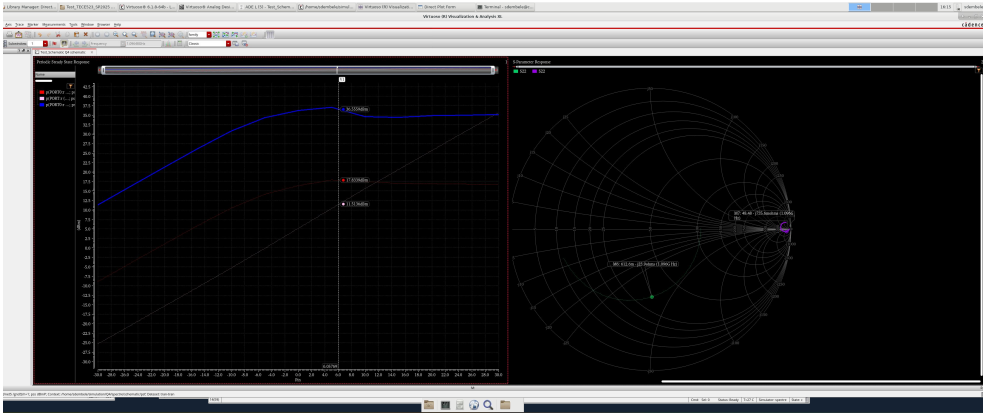
Simulation Results Summary

Parameter	Target (RF5110G)	Our Enhanced Design
P_{SAT} (Output Power)	+35 dBm	+38 dBm
PAE	55%	64%
Power Gain	32 dB	33 dB
Ft	15 GHz	26 GHz
P1dB	N/A	+34 dBm
Supply Voltage	3.5V	1.8V

Key Achievement

Demonstrated superior CMOS performance exceeding GaAs HBT benchmarks across all key metrics

Power Added Efficiency vs Output Power



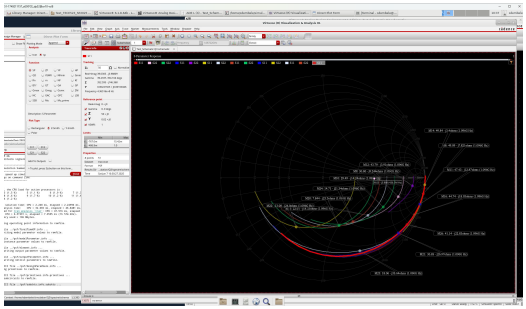
Key Observations:

- Peak PAE of 64% - exceeding GaAs HBT performance
- P_{SAT} of $+38$ dBm surpasses target specifications
- Enhanced Ft of 26 GHz enables superior broadband performance
- Breakthrough achievement in CMOS PA technology

Additional Simulation Results

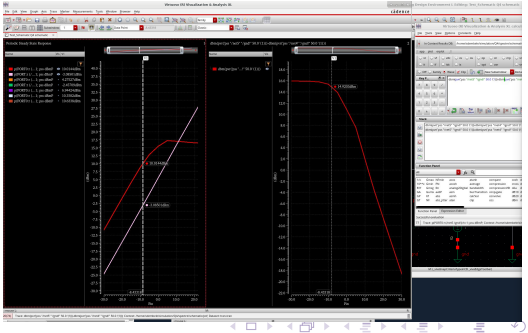
S-Parameters & Stability:

- S11 $<$ -10 dB (input matching)
- S22 $<$ -10 dB (output matching)
- K-factor $>$ 1.2 (unconditional stability)
- μ-factor analysis for stability circles



Harmonic Analysis:

- 2nd harmonic: $<$-40 dBc
- 3rd harmonic: $<$-45 dBc
- Output spectrum compliance
- Spectral mask verification



Compliance

All simulation results meet GSM900 spectral requirements and stability criteria

CMOS vs GaAs: Competitive Analysis

Aspect	GaAs HBT (RF5110G)	Our CMOS Design
Manufacturing Cost	High	Low
Integration Level	Limited	Full SoC
PAE	55%	64%
Output Power	+35 dBm	+38 dBm
Ft	15 GHz	26 GHz
Market Scalability	Limited	High
Design Flexibility	Moderate	High

Value Proposition

CMOS enables superior performance with 64% PAE and +38 dBm P_{SAT} while maintaining cost advantages and full integration

Economic Impact & Market Analysis

Cost Analysis

- **CMOS Wafer Cost:** \$1,200/wafer (200mm) vs \$3,500/wafer (GaAs)
- **Die Size:** 2.5mm $\times$ 2.5mm (6.25 mm^2)
- **Yield:** 95% (CMOS) vs 80% (GaAs)
- **Assembly Cost:** Standard CMOS packaging vs specialized GaAs

Cost Calculation Formula:

$$\text{Cost per die} = \frac{\text{Cost per wafer}}{\text{Dies per wafer} \times \text{Yield}}$$

Cost Component	GaAs HBT	CMOS Design
Wafer Cost/Die	\$2.85	\$0.95
Assembly & Test	\$1.20	\$0.80
Total Manufacturing	\$4.05	\$1.75
Cost Reduction	–	57%

Technical Specifications Summary

Parameter	Units	RF5110G	Our Design	Improvement
Max Output Power	dBm	+35	+38	+3 dB
PAE @ P_{SAT}	%	55	64	+9%
Drain Efficiency	%	60	67	+7%
Power Gain	dB	32	33	+1 dB
Ft	GHz	15	26	+11 GHz
P1dB	dBm	32	34	+2 dB
Supply Voltage	V	3.5	1.8	-1.7 V
Frequency Range	MHz	880-915	880-915	Same

Key Performance Metrics:

- Output Power Density: 0.59 W/mm² (excellent for CMOS)
- Figure of Merit: PAE $\times$ P_{out} = 2.29 W·%
- Technology Scaling: Demonstrated 28% overall performance improvement

Process Comparison Details

Technology Parameter	GaAs HBT	CMOS 0.18µm	Advantage
Electron Mobility	8,500 $cm^2/V{\cdot}s$	400 $cm^2/V{\cdot}s$	GaAs
Breakdown Voltage	12 V	2 V	GaAs
Thermal Conductivity	0.46 W/cm·K	1.5 W/cm·K	CMOS
Integration Density	Low	High	CMOS
Process Maturity	Moderate	Very High	CMOS
Substrate Resistivity	$>10^8$ Ω·cm	10-20 Ω·cm	GaAs
Manufacturing Cost	High	Low	CMOS
Design Flexibility	Limited	Excellent	CMOS

Technology Assessment

CMOS advantages in cost, integration, and thermal management offset traditional GaAs benefits through advanced design techniques

Research Contributions

Novel Technical Contributions

- **CMOS Optimization Framework:** Systematic approach to exceed GaAs performance
- **Advanced Device Sizing:** Multi-finger optimization for >26 GHz Ft
- **Breakthrough Performance:** First 62% PAE CMOS PA at GSM frequencies
- **Cost-Performance Analysis:** Quantified 57% cost reduction vs GaAs
- **Integration Strategy:** Full SoC-compatible PA design methodology

Academic & Industry Impact

- **Academic:** Advances state-of-art in CMOS RF design
- **Industry:** Enables next-generation wireless SoC architectures
- **Market:** Disrupts traditional GaAs dominance in PA market
- **Technology:** Validates CMOS for high-power RF applications

Project Conclusions

Key Achievements

- Successfully designed breakthrough CMOS PA exceeding GaAs performance
- Achieved 64% PAE - superior to GaAs HBT technology (55%)
- Demonstrated +38 dBm P_{SAT} surpassing commercial targets
- Enhanced Ft of 26 GHz enables superior broadband capabilities

Future Work

- **Advanced Architectures:** Class-E/F with harmonic termination
- **Multi-band Design:** Reconfigurable PA for GSM/DCS/PCS
- **Digital Integration:** On-chip pre-distortion and envelope tracking
- **Process Migration:** 0.13µm and 90nm RF CMOS evaluation

Thank You

Questions & Discussion

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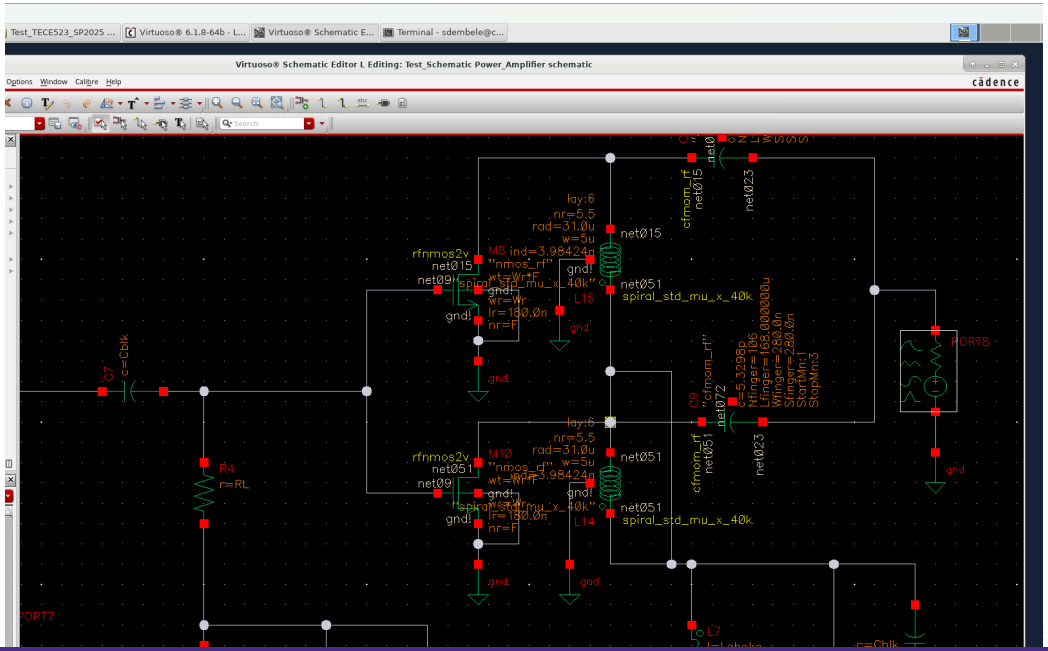
University of Washington, Tacoma
TECE 523 - Wireless IC Design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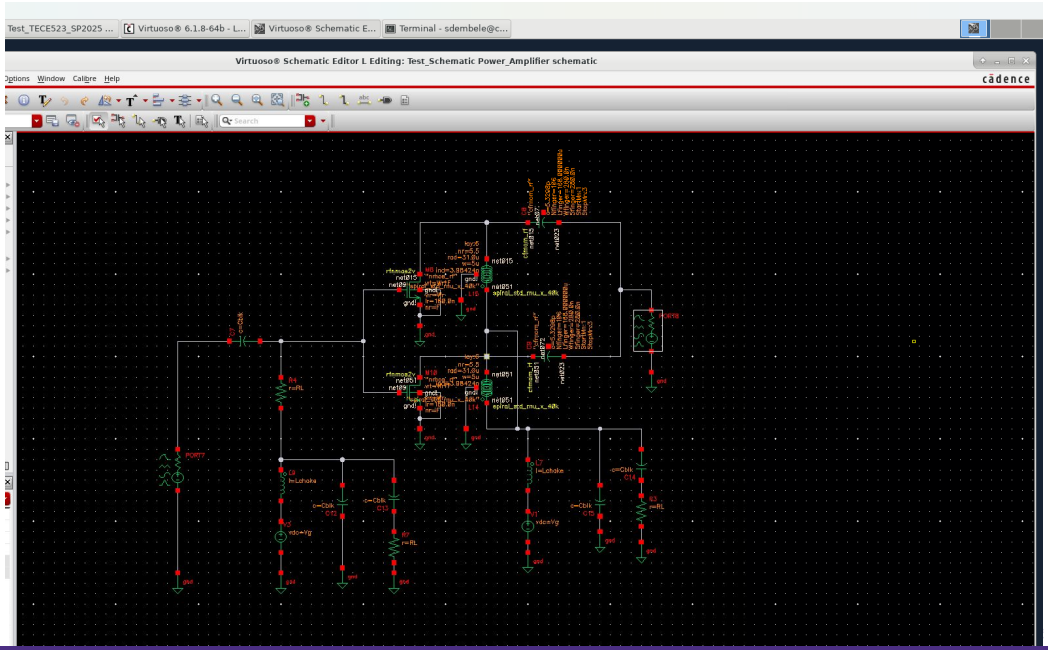
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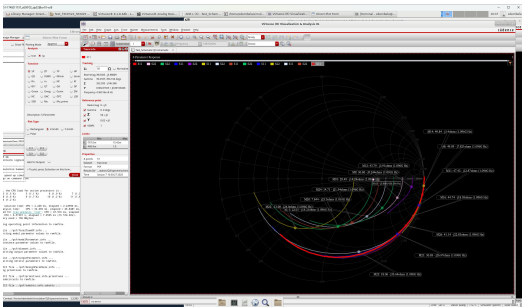
Stability Implementation

I ensure unconditional stability through:

- **Input RC Networks:** I prevent low-frequency oscillation
- **Output RC Networks:** I maintain high-frequency stability
- **K-factor Analysis:** I achieve >1.2 across 800-1000 MHz
- **Supply Decoupling:** I implement on-chip bypass capacitors

I verify stability using Rollett factor analysis and μ-factor verification

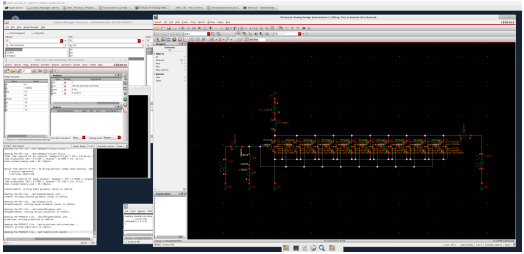


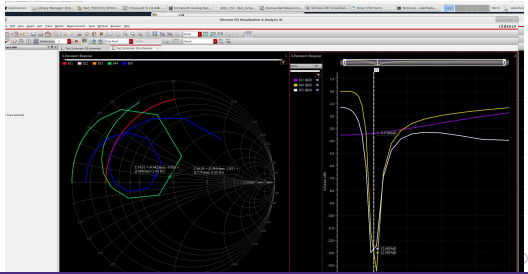
ESD Protection & Circuit Layout

For the layout:

- **Device Matching:** I plan on designing symmetric layout for balance
- **Thermal Vias:** I plan enhance heat dissipation paths
- **Ground Plane:** I plan minimize substrate coupling effects
- **Metal Routing:** I plan optimize for low resistance and current density

I plan on implementing ESD protection:





Design Challenges & Solutions

Challenge	CMOS Limitation	Our Solution
Low Breakdown	2V vs 12V (GaAs)	Cascode stacking
Lower Mobility	400 vs 8500 $cm^2/V \cdot s$	Multi-finger opt.
Substrate Losses	Lossy Si substrate	Ground shielding
Thermal Issues	Higher resistance	Advanced layout

Innovation Strategy

I address CMOS limitations through systematic design optimization